

# EdgeTunePower

Importance of Real-time Simulation and HIL  
Testing for De-risking Operation of Data Centres

Arman Ghasaei, Ph.D., CTO

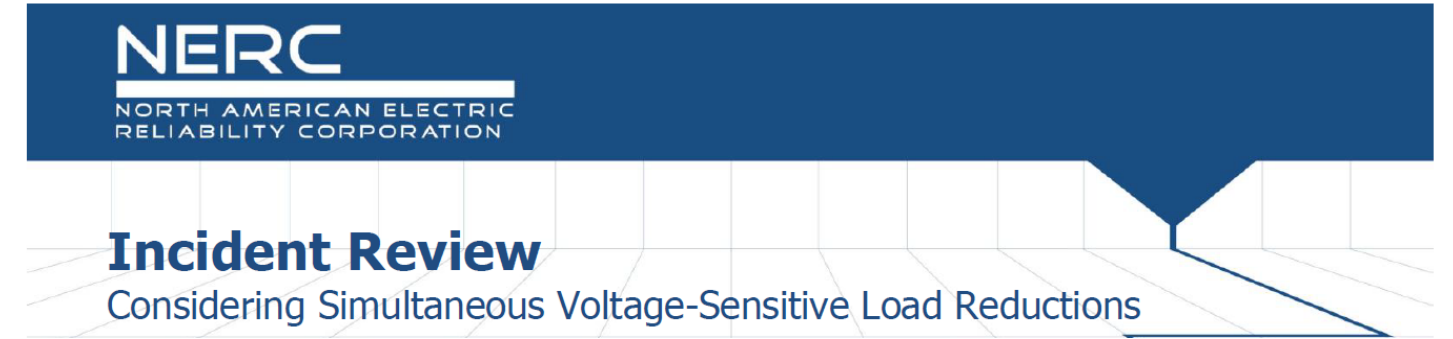
# Agenda

- Problem statement
- What is HIL Testing
- Which devices can be tested for Data Centres with HIL Approach
- Results and Lessons Learned from a 20-MW Data Centre project

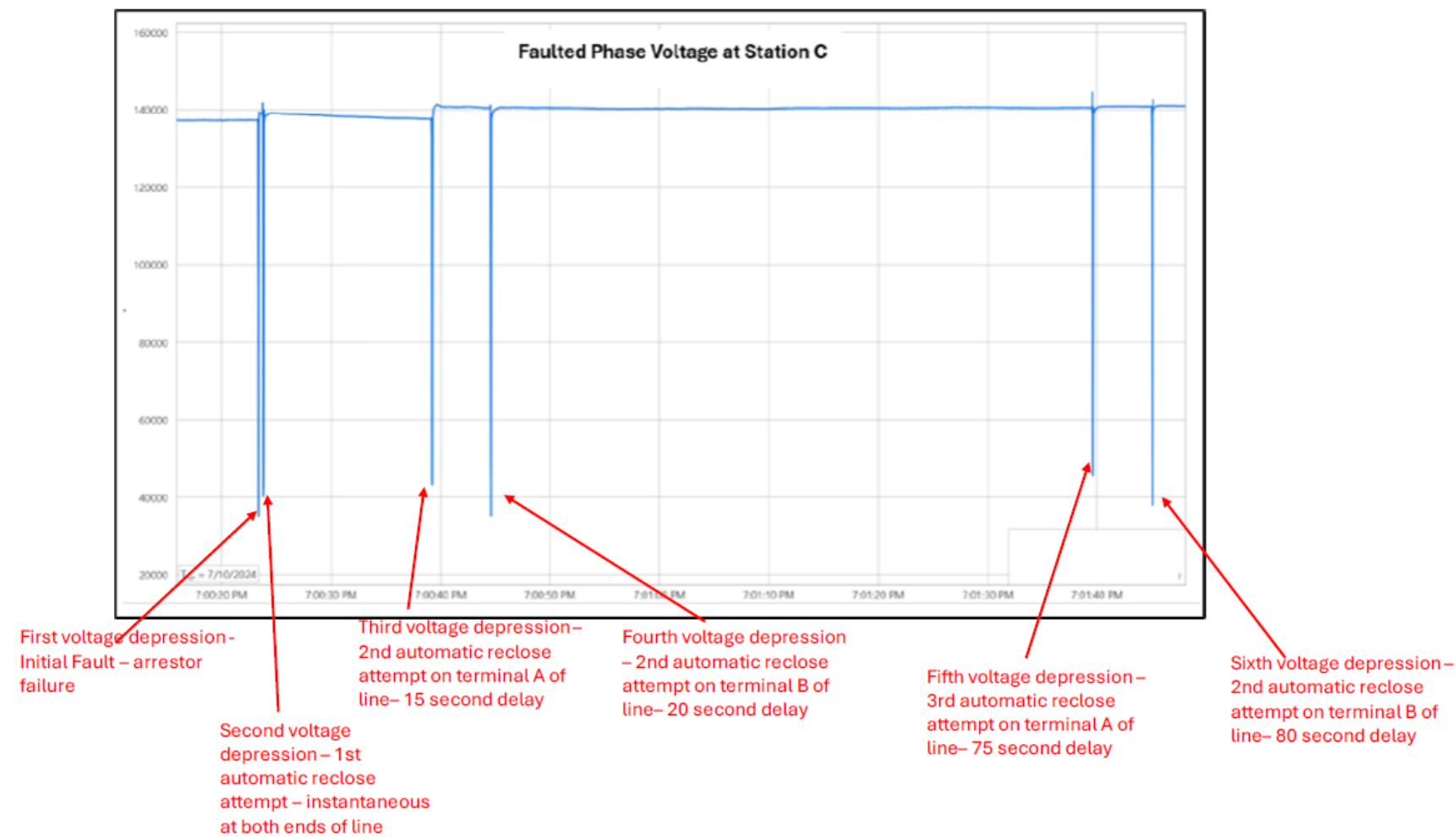


# Problem Statement:

- **Rising Risk** – Growing voltage-sensitive loads increase future reliability and reconnection challenges!



- 2024: Large Load Loss – 230-kV fault caused ~1,500 MW data center load drop, risking frequency/voltage swings.



- Reclosing Interaction – Reclose attempts triggered protection logic, keeping ~1,260 MW offline for hours!!!

# Co-location of Data Centres with Power Plants.

## However, even in power plants:

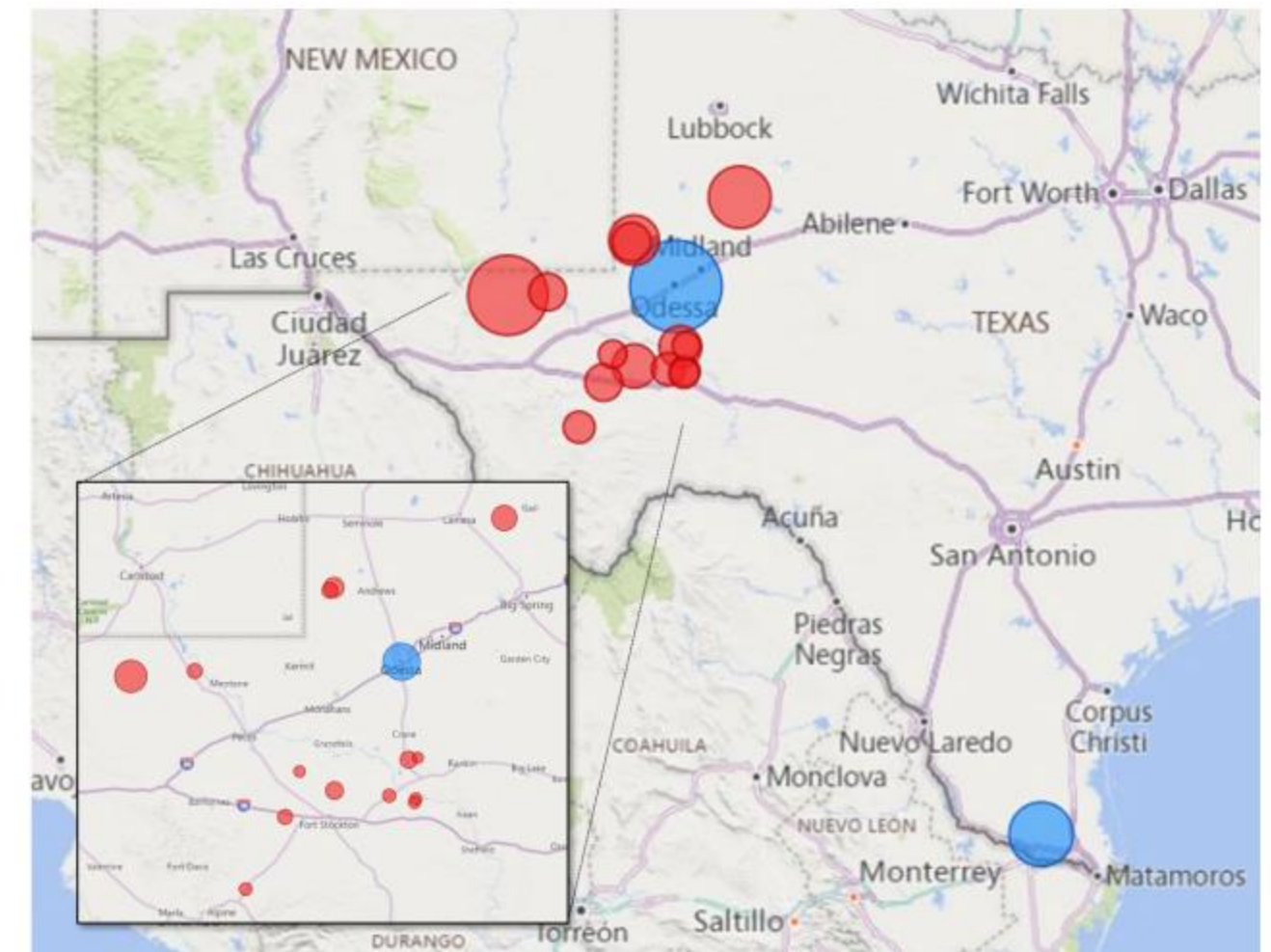
✗ Some IBR-dominated plants are not behaving reliably!

✗ Mal-operational **Physical** control systems, at IBR level and system level (PPC), during field operation

!! **Physical** control systems need to be tested in advance

!! Odessa Event 2021: **1.1 GW** solar-PV reduction after a S-L-G fault

!! Odessa Event 2022: : **1.7 GW** solar-PV reduction after a S-L-G fault



## Root cause:

✘ Mal-operation of control systems (IBRs and PPC) despite offline simulations and modeling

ODESSA 2021	ODESSA 2022
PLL Loss of Synchronism: <b>389 MW</b> reduction.	Inverter Instantaneous AC Overcurrent: <b>445 MW</b> reduction.
Inverter AC Overvoltage: <b>269 MW</b> reduction	Voltage Phase Jump: <b>385 MW</b> reduction.
Momentary Cessation: <b>153 MW</b> reduction	Inverter AC Overvoltage: <b>295 MW</b> reduction.
Feeder AC Overvoltage: <b>147 MW</b> reduction	Inverter DC Bus Unbalance: <b>198 MW</b> reduction.
Inverter Underfrequency: <b>48 MW</b> reduction	Slow Ramp After Low Voltage Ride Through (LVRT): <b>147 MW</b> reduction.
Other/Unknown Causes: <b>85 MW</b> reduction	Momentary Cessation: <b>131 MW</b> reduction.
	Grid Over frequency: <b>50 MW</b> reduction.
	Other/Unknown Causes: <b>59 MW</b> reduction.

Source: ERCOT

# Root cause:

## ✗ Communication Latency!

<u>Protocol</u>	<u>Typical Latency</u>
Goose (IEC 61850)	<u>3 ms</u>
Modbus RTU	<u>20–100 ms</u>
Modbus TCP	<u>10–50 ms</u>
DNP3 (Serial)	<u>50–200 ms</u>
DNP3 (Ethernet)	<u>20–100 ms</u>
MMS (IEC 61850)	<u>10–100 ms</u>

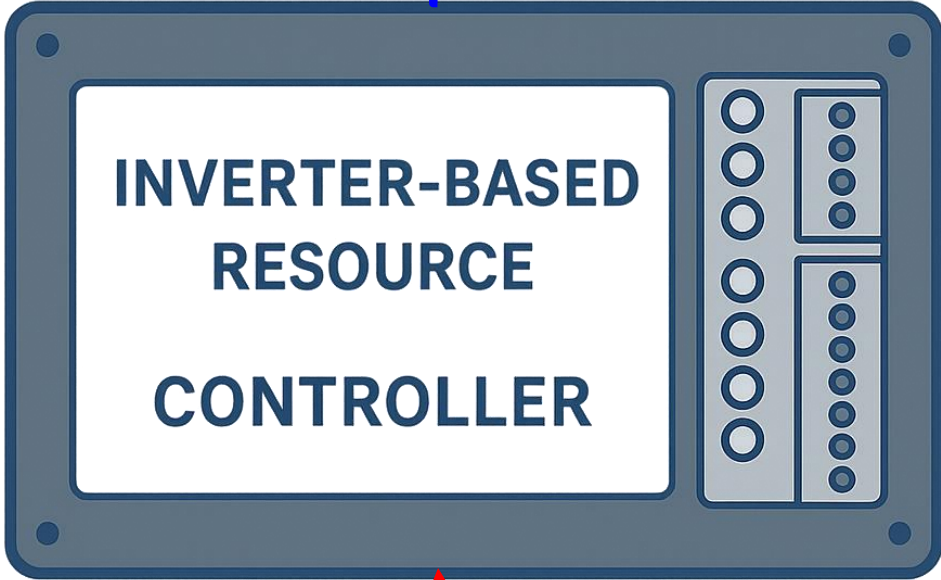
Source: SEL, IEEE

# C-HIL for an IBR Controller



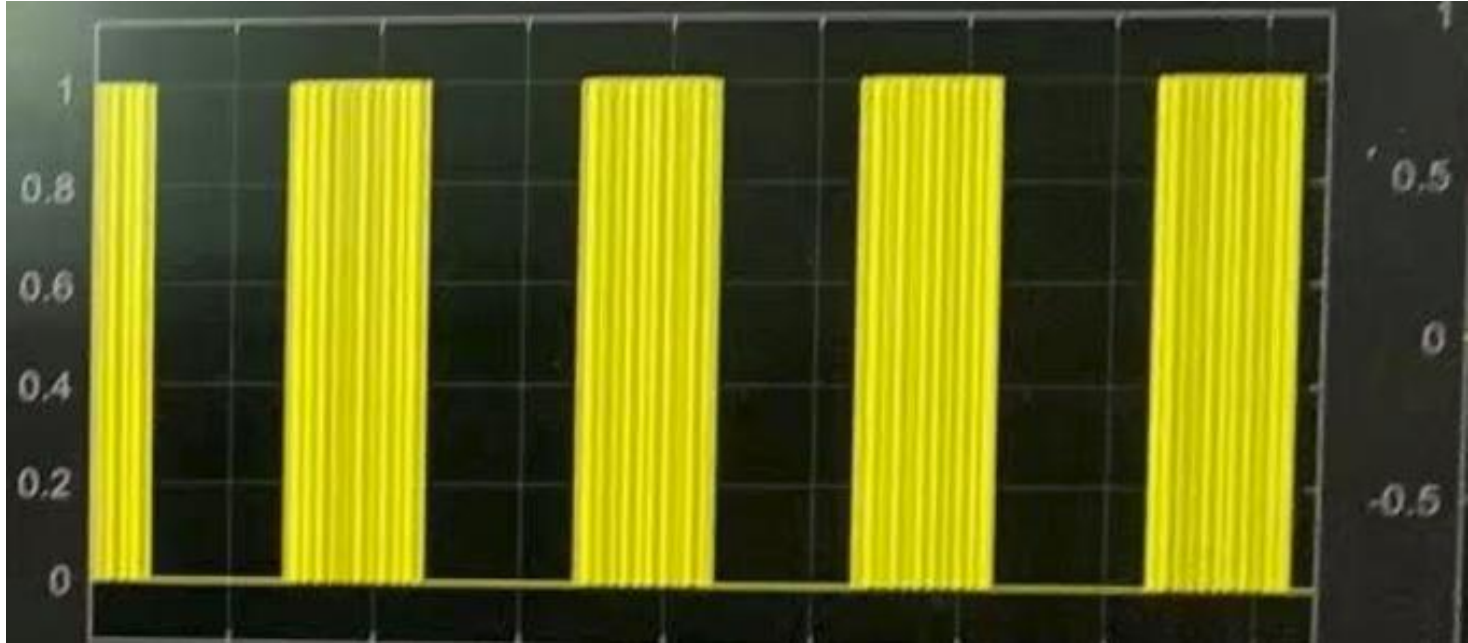
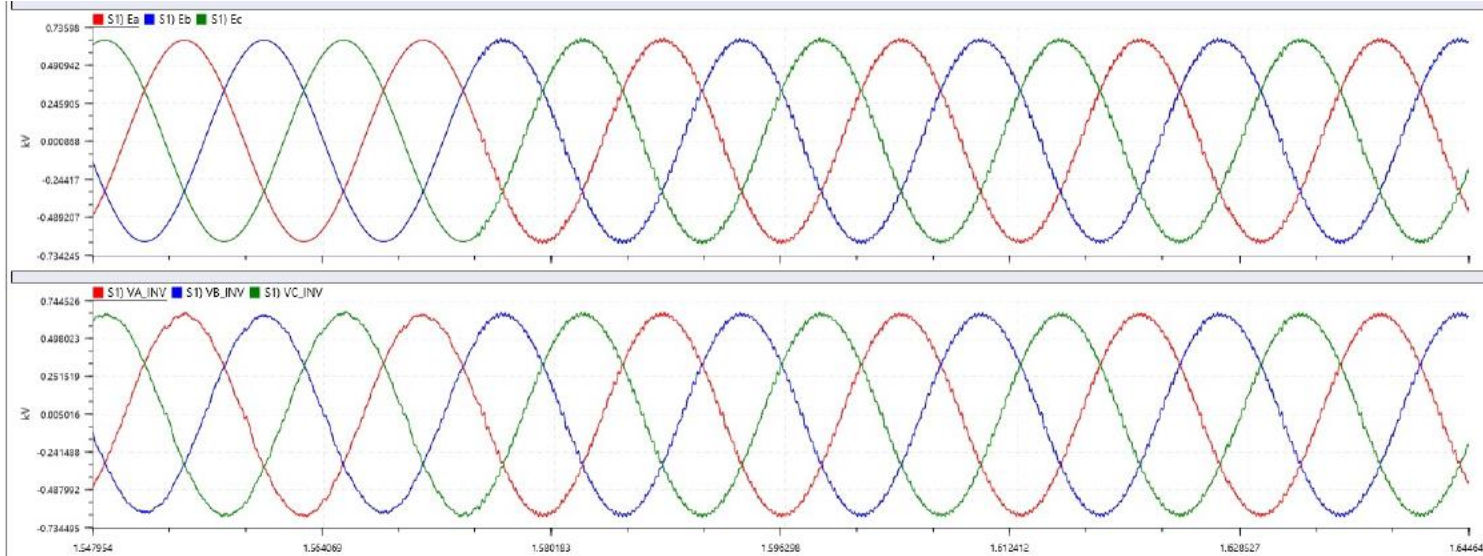
Real-time Digital Simulator

**Analog Voltage & Current (+-10V)**



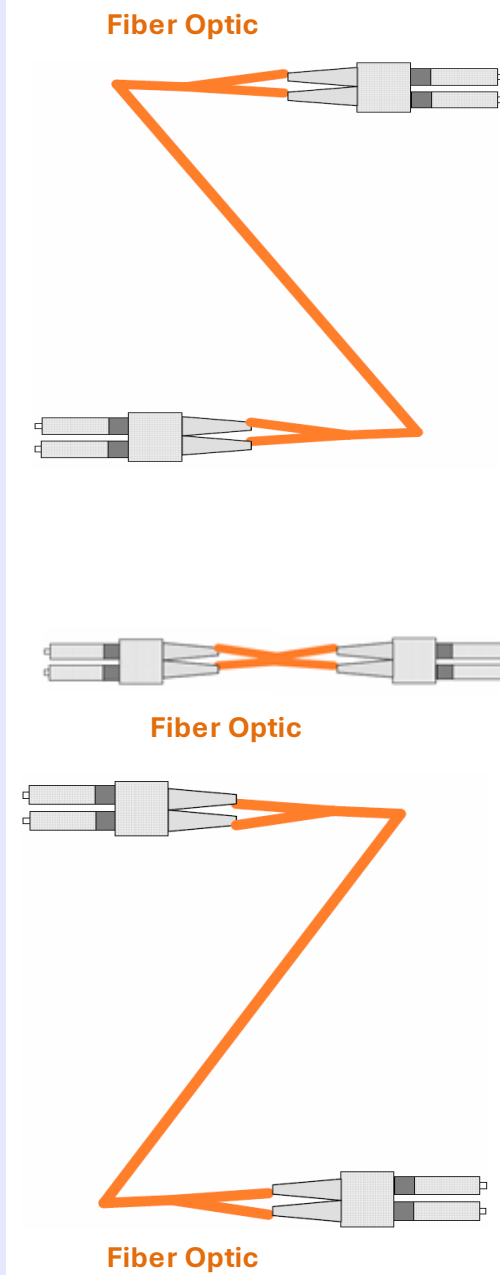
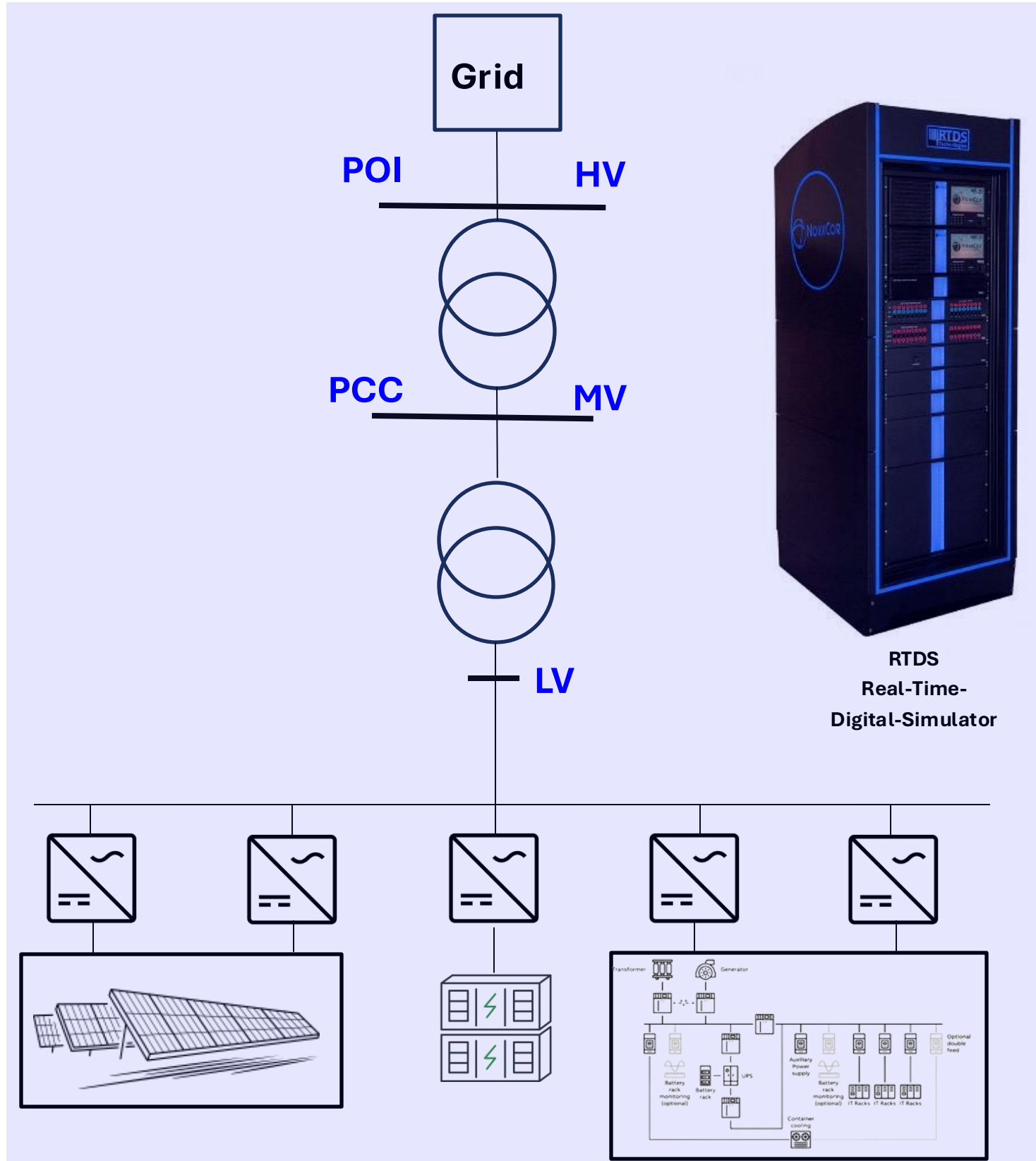
IBR Control System (This is the OEM controller)

**Digital Firing Pulses (+-24V)**



# Comprehensive HIL Structure

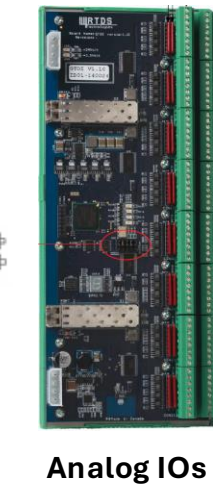
EMS+PMS+PPC



Communication  
(IEC-61850, MODBUS, DNP3)

IEEE C.37.118  
Synchrophasor

Voltage & Current  
(HV, MV, LV)



Firing Pulses

Communication  
(IEC-61850)

Protection & Meters



Communication  
(IEC-61850)

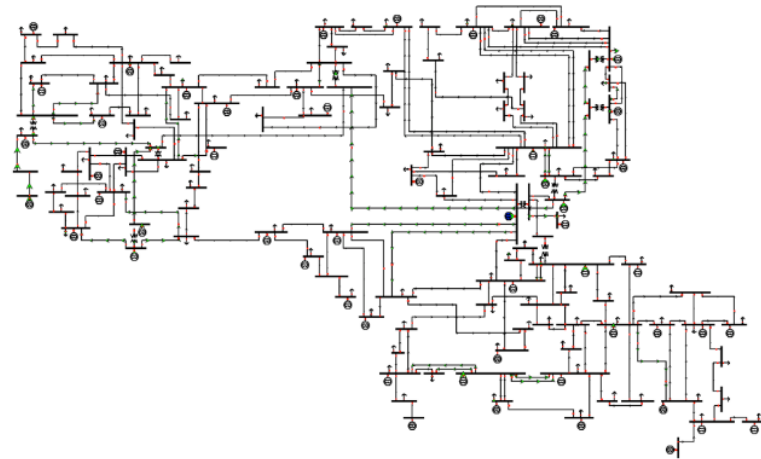


PCS Controller

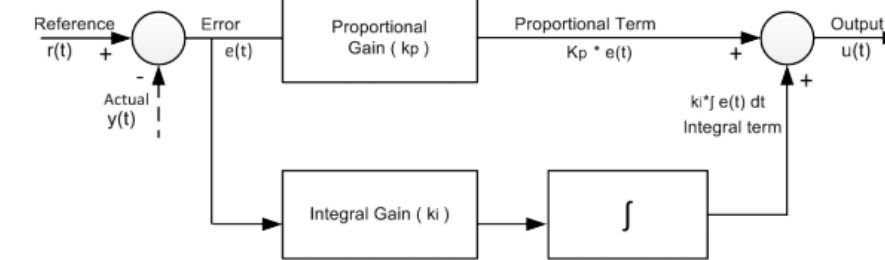
MODBUS  
DNP3

# Importance of HIL

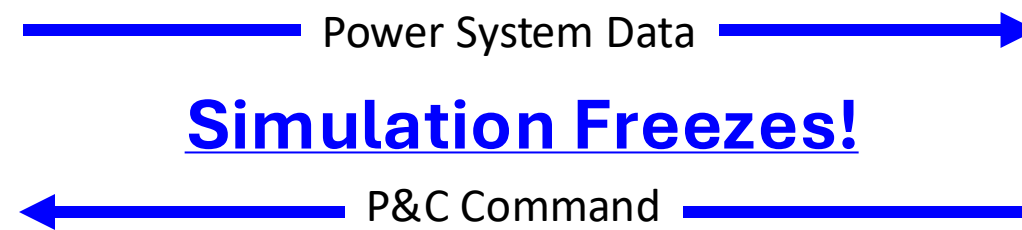
## Power System/ Data Centre Model



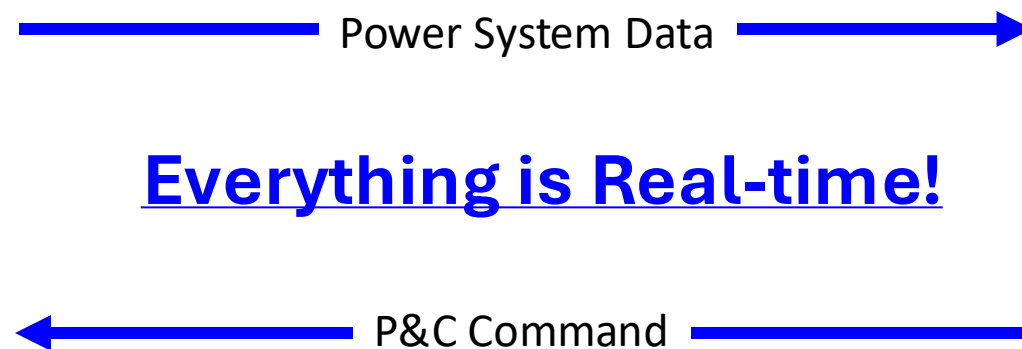
## Control/Protection System



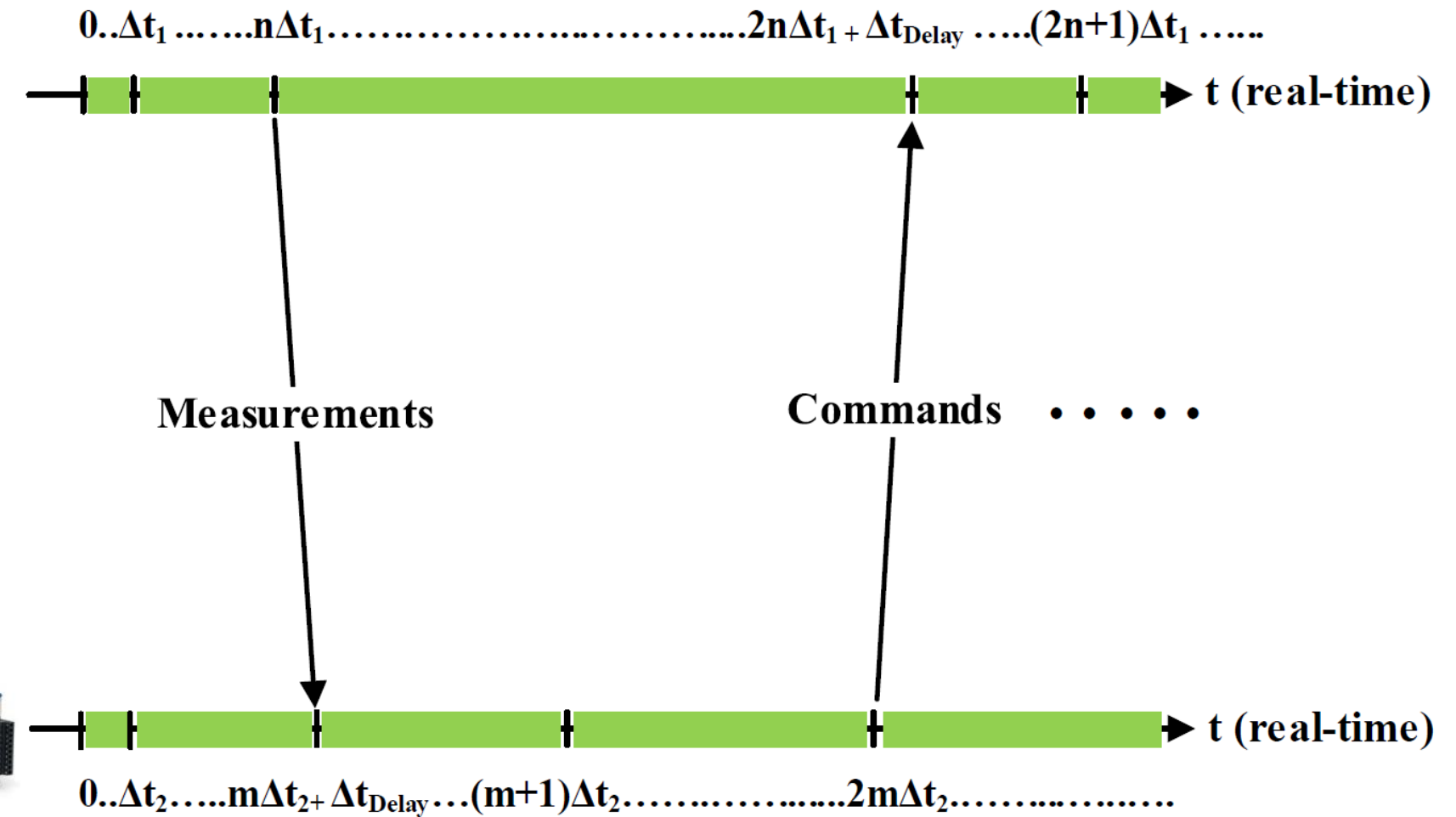
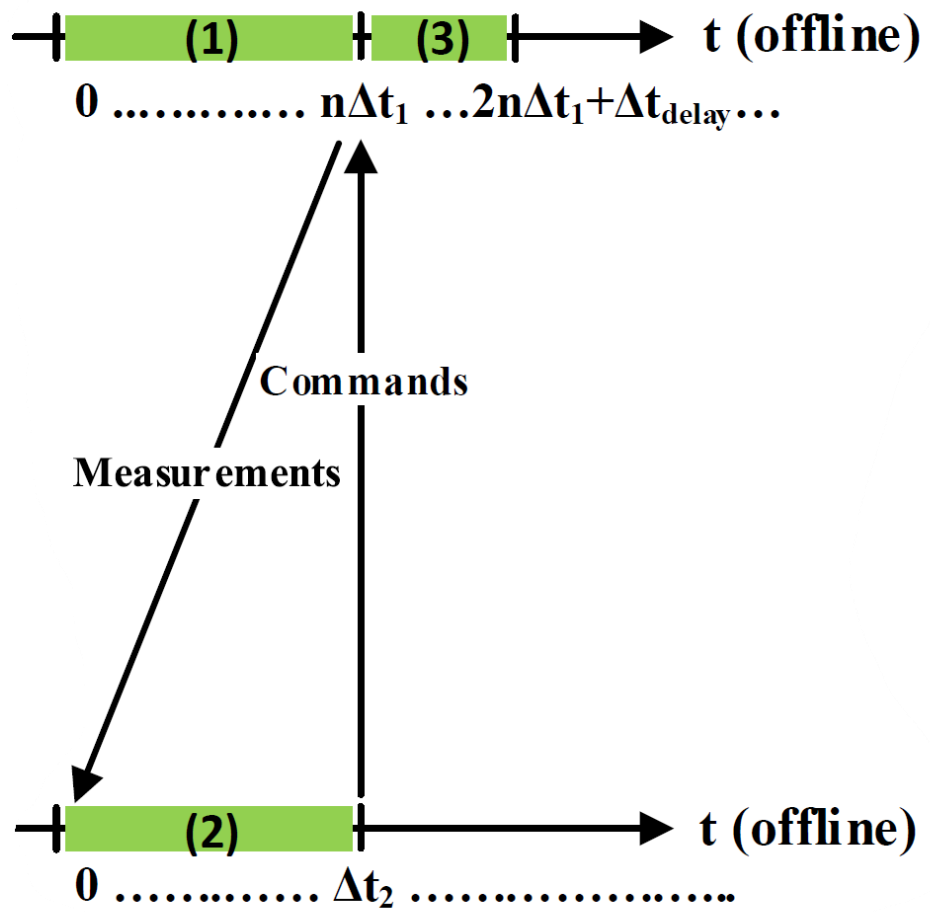
**Offline:**



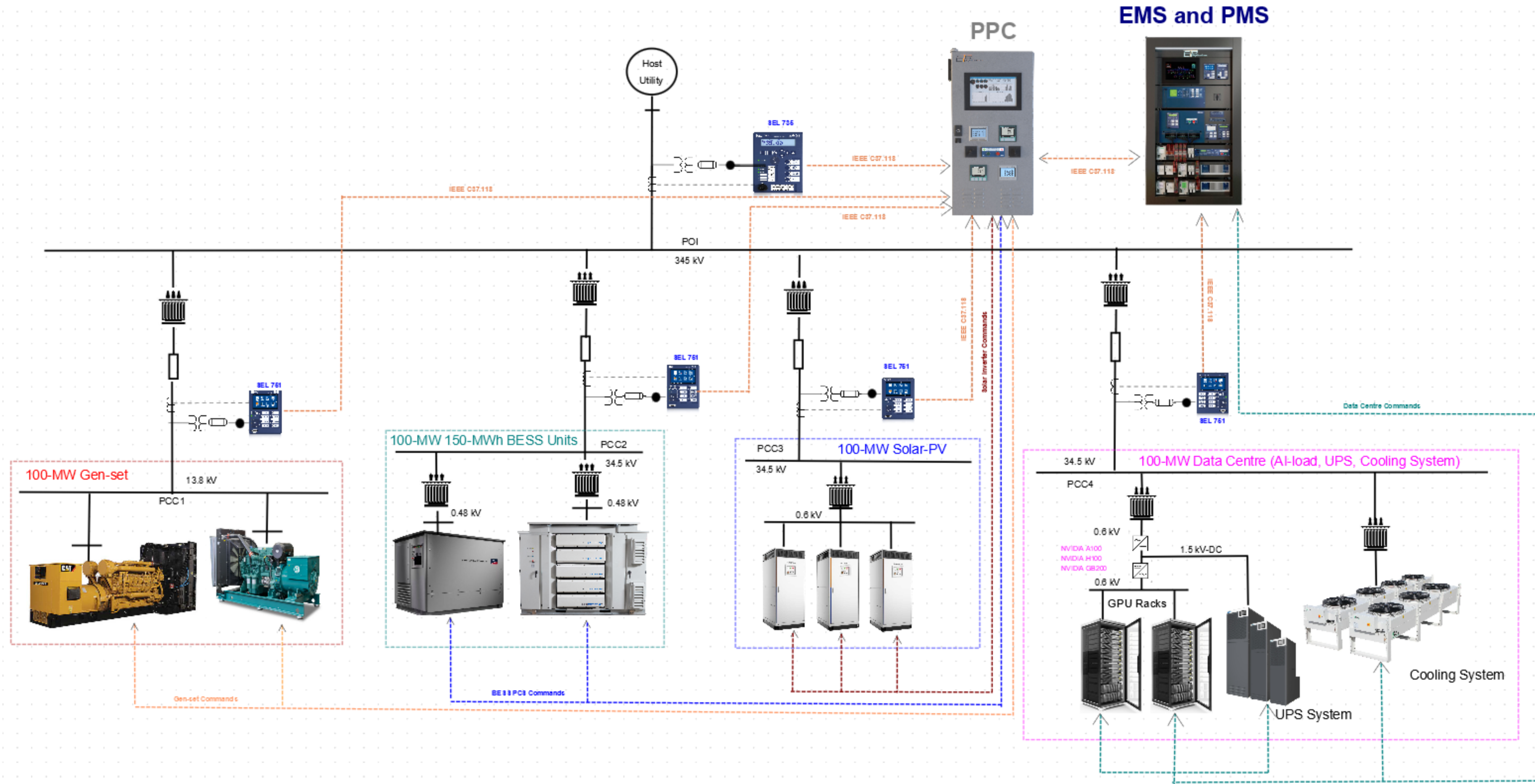
**Realtime  
(HIL):**



# Difference with Conventional Simulation



# Data Center Test-bed and AI load Simulator



# Digital Twin

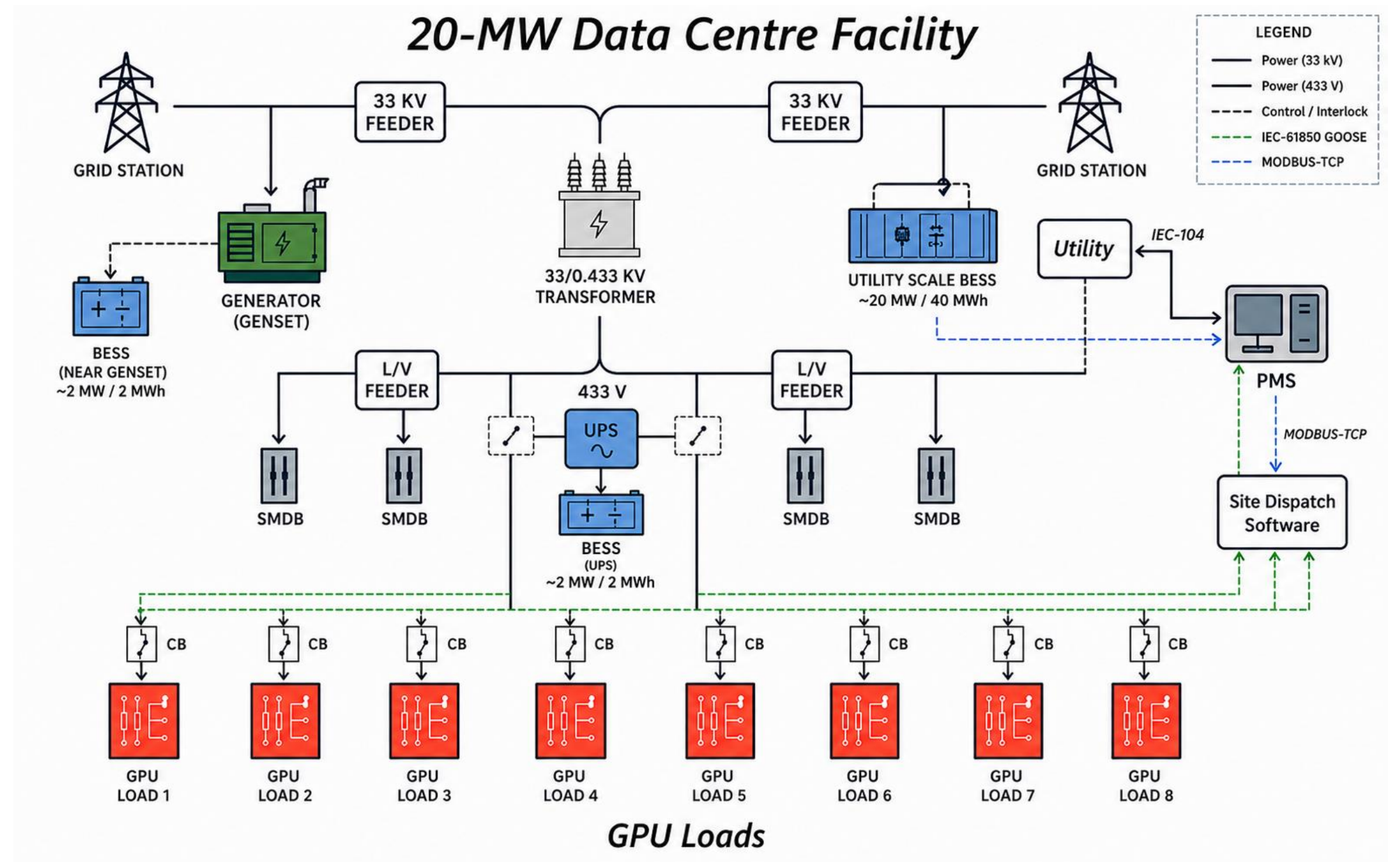
## De-Risk Commissioning and HIL Testing

- PCS, IBR Control Systems
- PPC, PMS, EMS via IEEE C37, MODBUS, DNP3, and IEC 61850
- Test and Validate controllers, protection, and communication



# Data Centre Facility

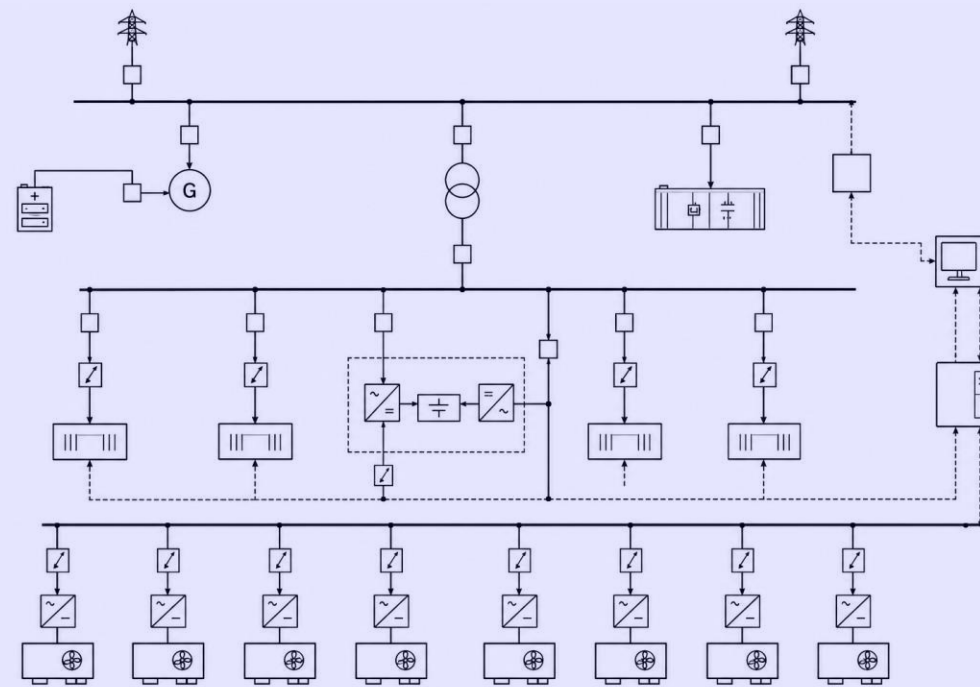
Link	Protocol
UTILITY ↔ PMS (ETP)	IEC-104
PMS (ETP) ↔ Site Dispatch Software Between GPUs	Modbus-TCP
Site Dispatch Software ↔ GPU Systems	Ethernet (Modbus-TCP)
PMS (ETP) ↔ CBs Connecting GPUs	IEC-61850 (GSE)



# HIL Testing of Dema Data Centre Facility

## IEC-104 Emulator for Utility

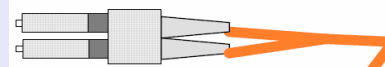
SNo	Server IP Address	Port	Common Address	Event Report Type Id	IDM...	Value...	Quality Bits	Time Stamp	IEC104 COT Cause	Control Model	ISO Time
1	192.168.2.11	2454	1	HLSP_MH_1	37	0.000	00	8:12:7:551 - 08/19/2025 HH:MM	PRCHYC	STATUS_OKAY	0
2	192.168.2.11	2454	1	HLSP_MH_1	38	0.000	00	8:12:7:551 - 08/19/2025 HH:MM	PRCHYC	STATUS_OKAY	0
3	192.168.2.11	2454	1	HLSP_MH_1	39	0.000	00	8:12:7:551 - 08/19/2025 HH:MM	PRCHYC	STATUS_OKAY	0
4	192.168.2.11	2454	1	HLSP_MH_1	40	0.000	00	8:12:7:551 - 08/19/2025 HH:MM	PRCHYC	STATUS_OKAY	0
5	192.168.2.11	2454	1	HLSP_MH_1	41	0.000	00	8:12:7:551 - 08/19/2025 HH:MM	PRCHYC	STATUS_OKAY	0
6	192.168.2.11	2454	1	HLSP_MH_1	42	0.000	00	8:12:7:551 - 08/19/2025 HH:MM	PRCHYC	STATUS_OKAY	0
7	192.168.2.11	2454	1	HLSP_MH_1	30	0	00	8:12:8:25 - 02/10/2025 HH:MM	PRCHYC	STATUS_OKAY	0
8	192.168.2.11	2454	1	HLSP_MH_1	31	0	00	8:12:8:25 - 02/10/2025 HH:MM	PRCHYC	STATUS_OKAY	0
9	192.168.2.11	2454	1	HLSP_MH_1	36	0.000	00	8:8:37:896 - 08/19/2025 HH:MM	PROGEN	STATUS_OKAY	0
10	192.168.2.11	2454	1	HLSP_MH_1	33	0	00	8:8:43:814 - 08/19/2025 HH:MM	PROGEN	STATUS_OKAY	0



RTDS  
Real-Time-  
Digital-Simulator



Fiber Optic



Fiber Optic



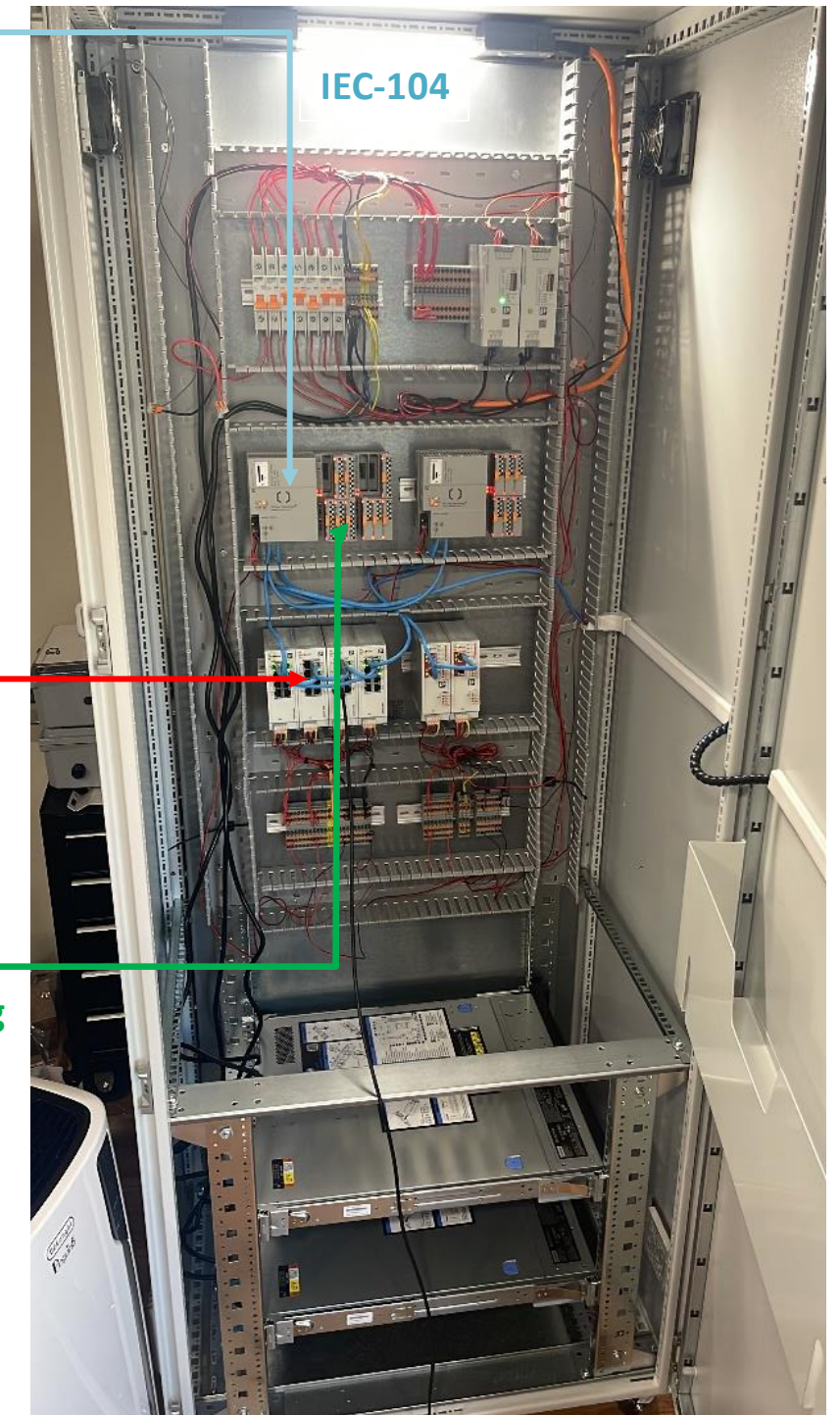
Network Card

MODBUS TCP



Digital IOs

Digital Load Shedding  
Commands



# Finding Issues with PCS Controller!



Figure 17. Installation of the film capacitor inside the ~~XXXXXXXXXX~~

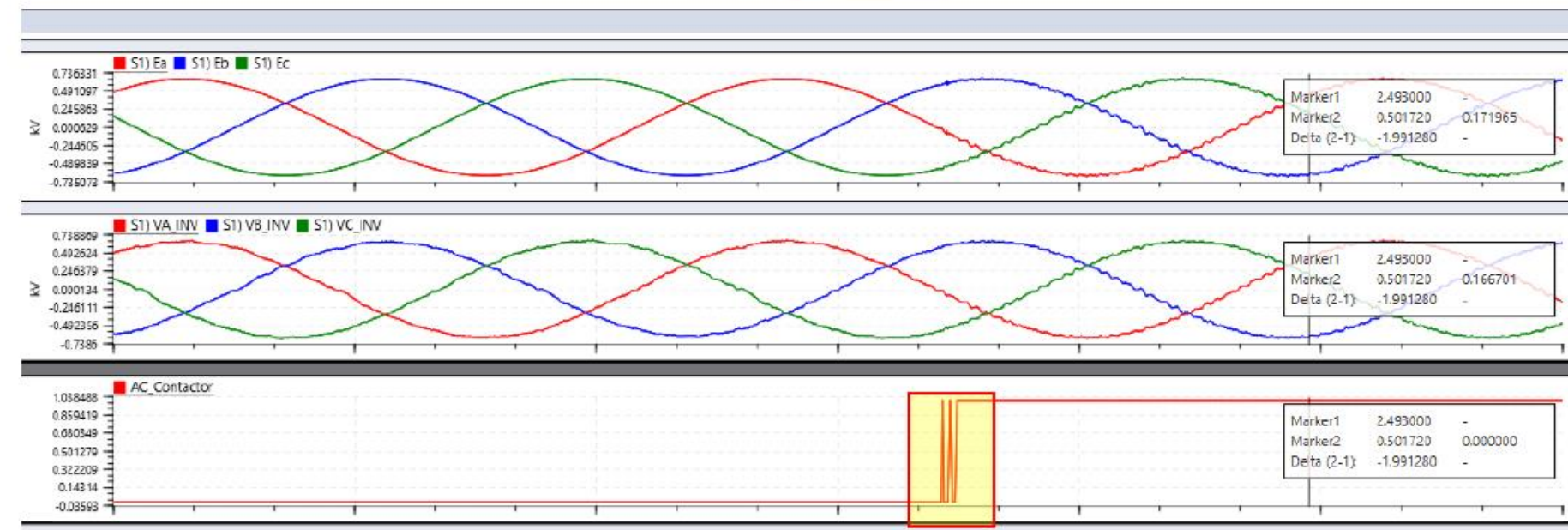
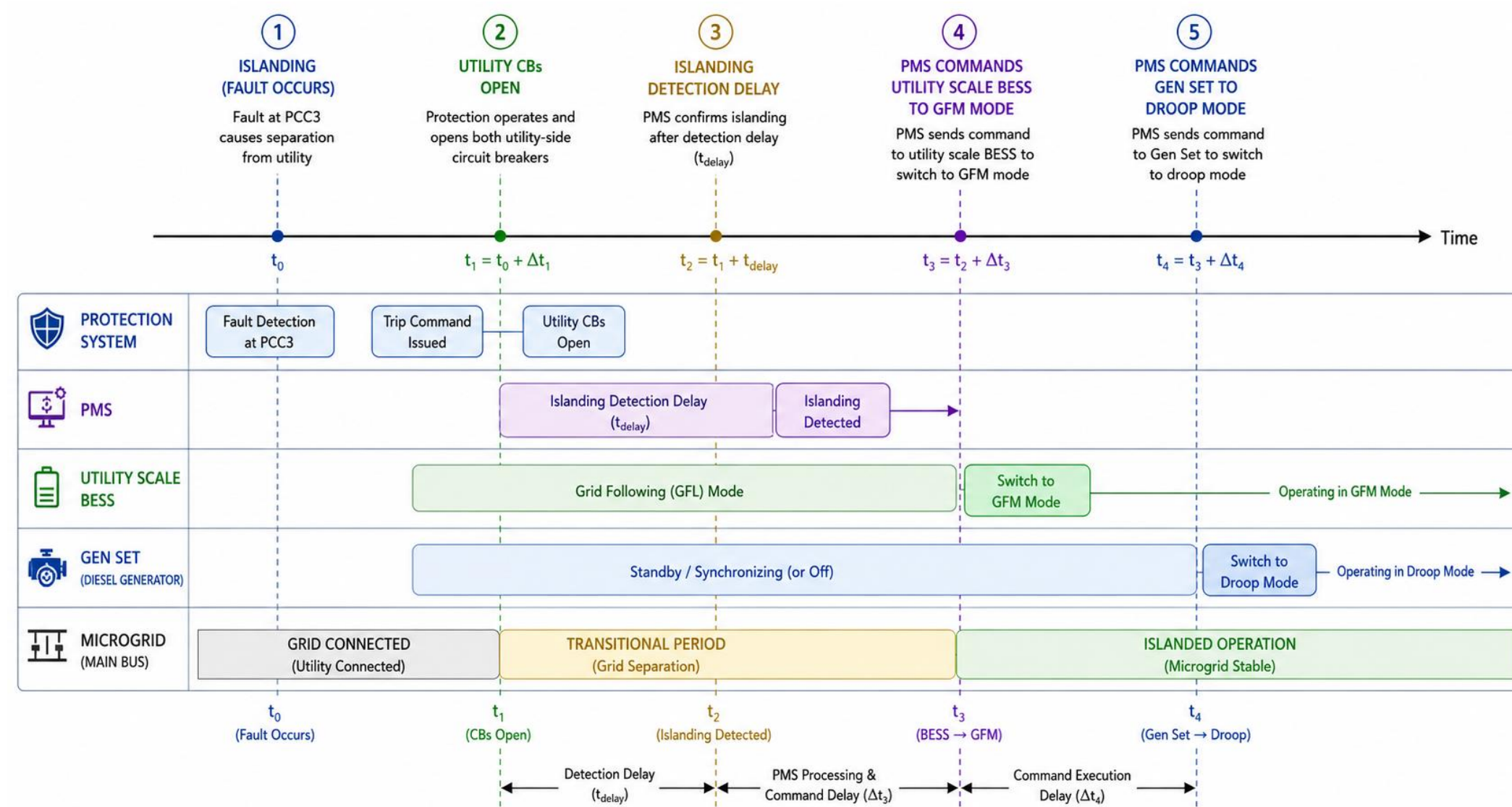
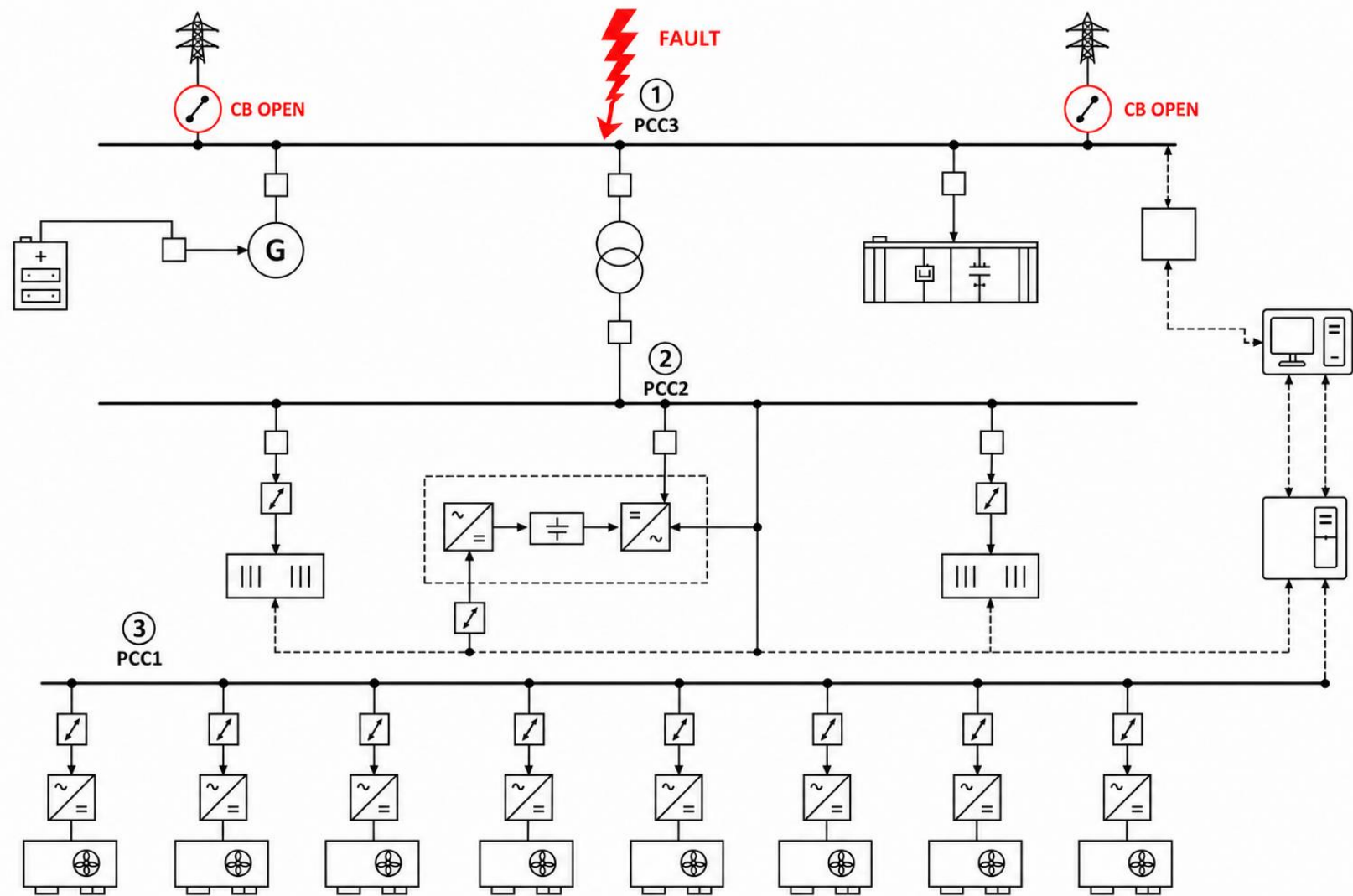


Figure 18. Jittering is observed in the status of the CB breaker

# System performance subsequent to accidental islanding



# System performance subsequent to accidental islanding

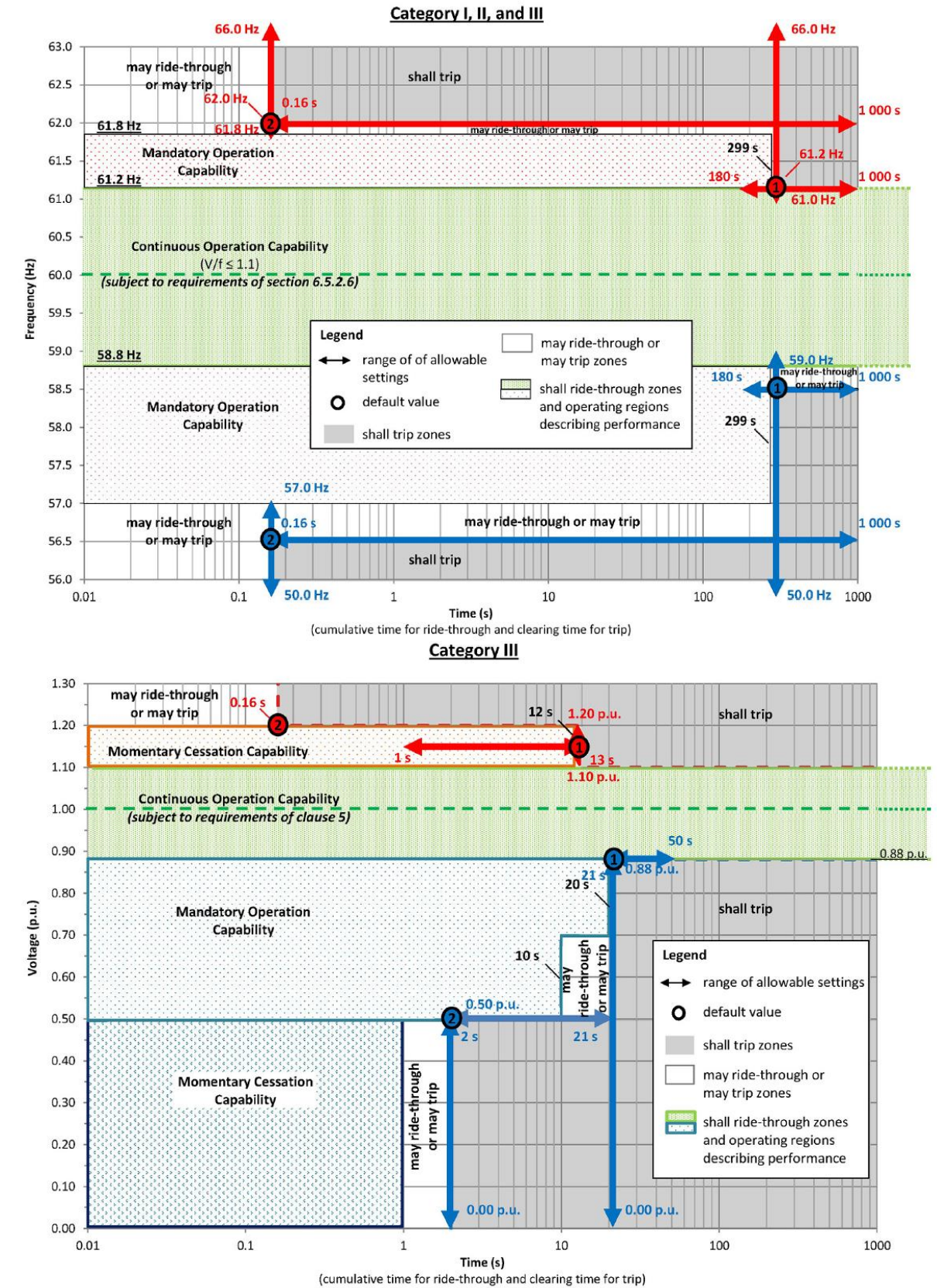
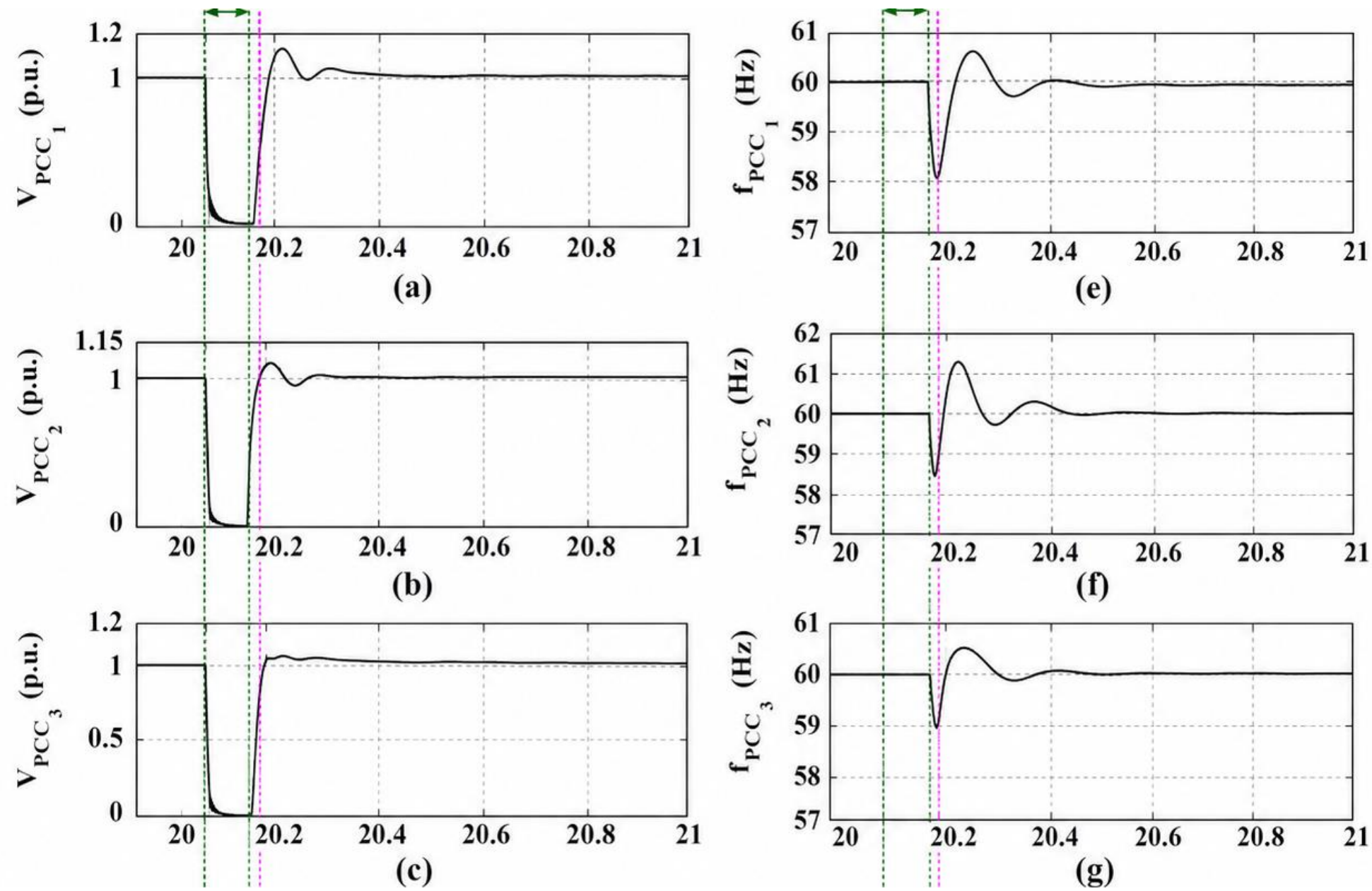
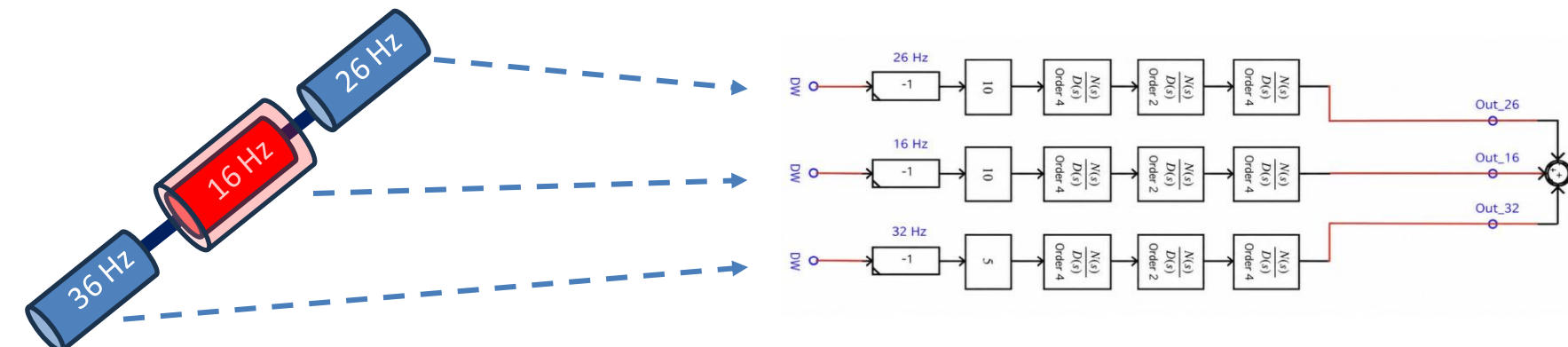
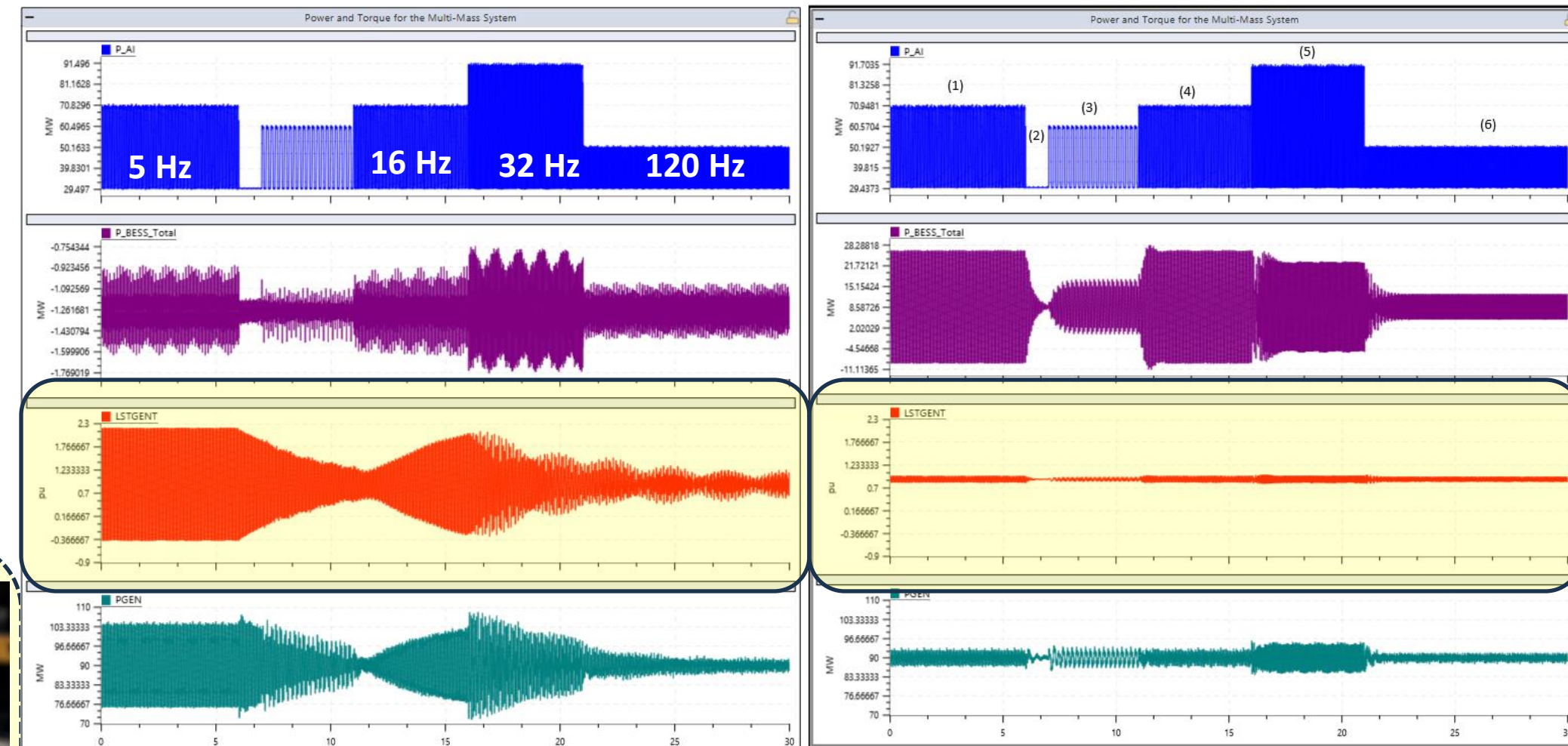
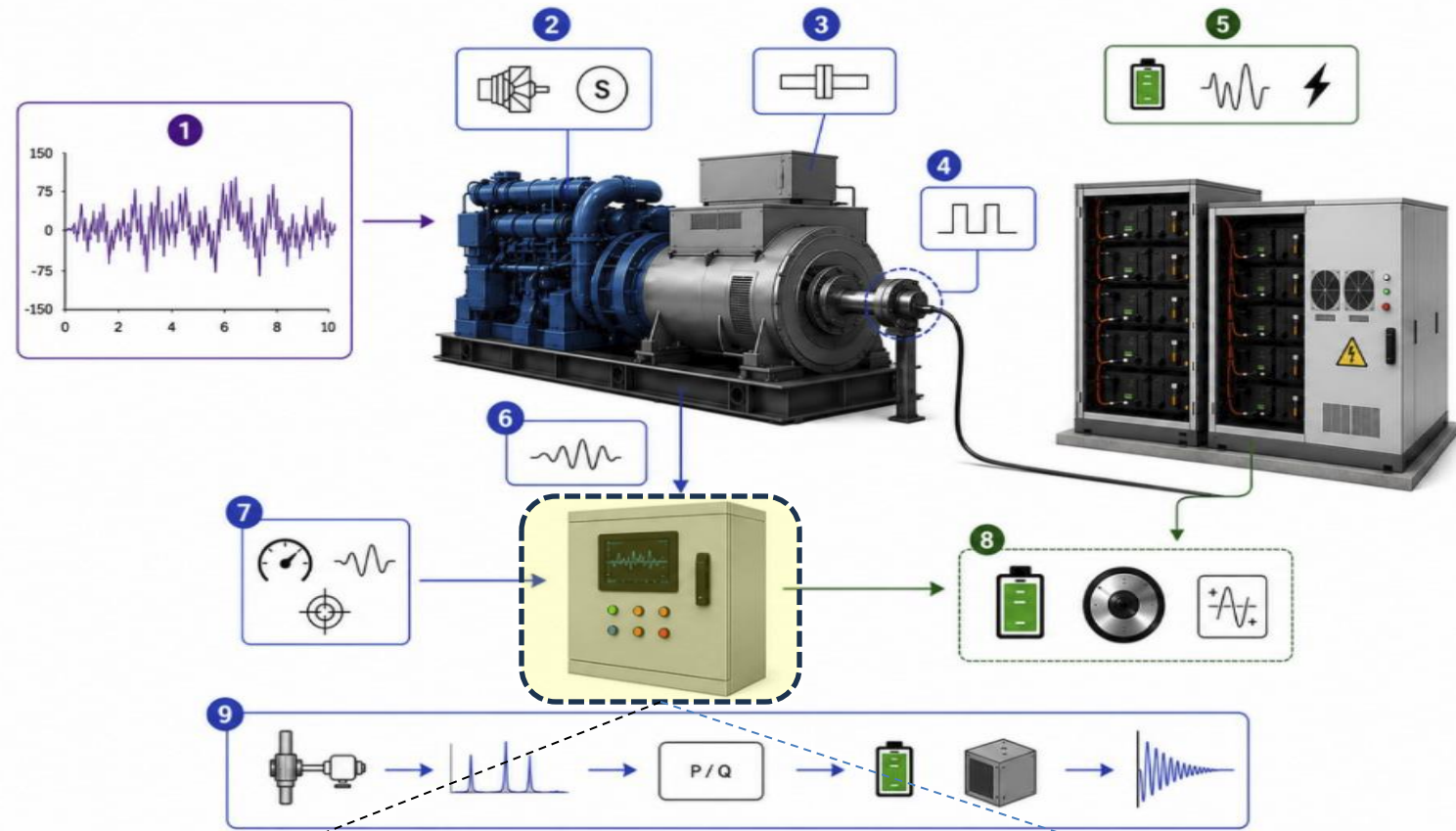


Figure H.9—DER response to abnormal voltages and voltage ride-through requirements for DER of abnormal operating performance Category III

# Novel Solution for SSTI Damping

## Advantages

- No Communication Latency
- Targeted Shaft Frequencies
- Only ~20% of the generator size for BESS



# THANK YOU