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Leveraging Hardware-in-the-Loop (HIL) Testing to Improve Model Fidelity and Accuracy

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ESIG Fall 2025 Workshop Panel Session: Importance of In-The-Loop Testing for Model Validation

About OPAL-RT TECHNOLOGIES

Founded in 1997

85% of customers in Power Systems and Power Electronics

Head office in Montréal

OPAL-RT TECHNOLOGIES

20% of annual revenue re-invested in R&D

1000+ customers around the world

Real-time simulators to design and test control systems

11
Offices

400+
Employees


Microgrid


Power Generation


Power System Controls


Wide Area Monitoring


Cybersecurity


Modular Multi-Level Converter (MMC)


Protection System


All Electric Ship


Battery Management System


Electric Vehicles

Intelligent vehicles


Aerospace and Defense

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Introduction

- Rapid proliferation and interconnection of IBRs and large loads (e.g., data centers, crypto mining facilities, etc.,) is altering the grid dynamics and introducing faster interactions, some of which have not been captured by existing models.
- Recent disturbance reports from NERC (e.g., Odessa reports) highlight several inadequacies in unit model validation, factory acceptance testing, as well as in model quality testing protocols.
- These include several factors such as incorrect settings/parameters and failure to appropriate model specific control/protection behaviors.
- Lack of adequate testing during the interconnection process leads to expensive delays during commissioning costing several thousands of dollars per day in liquidated damages.
- **Hardware-in-the-Loop (HIL) Testing is critical to ensure proper model validation!**

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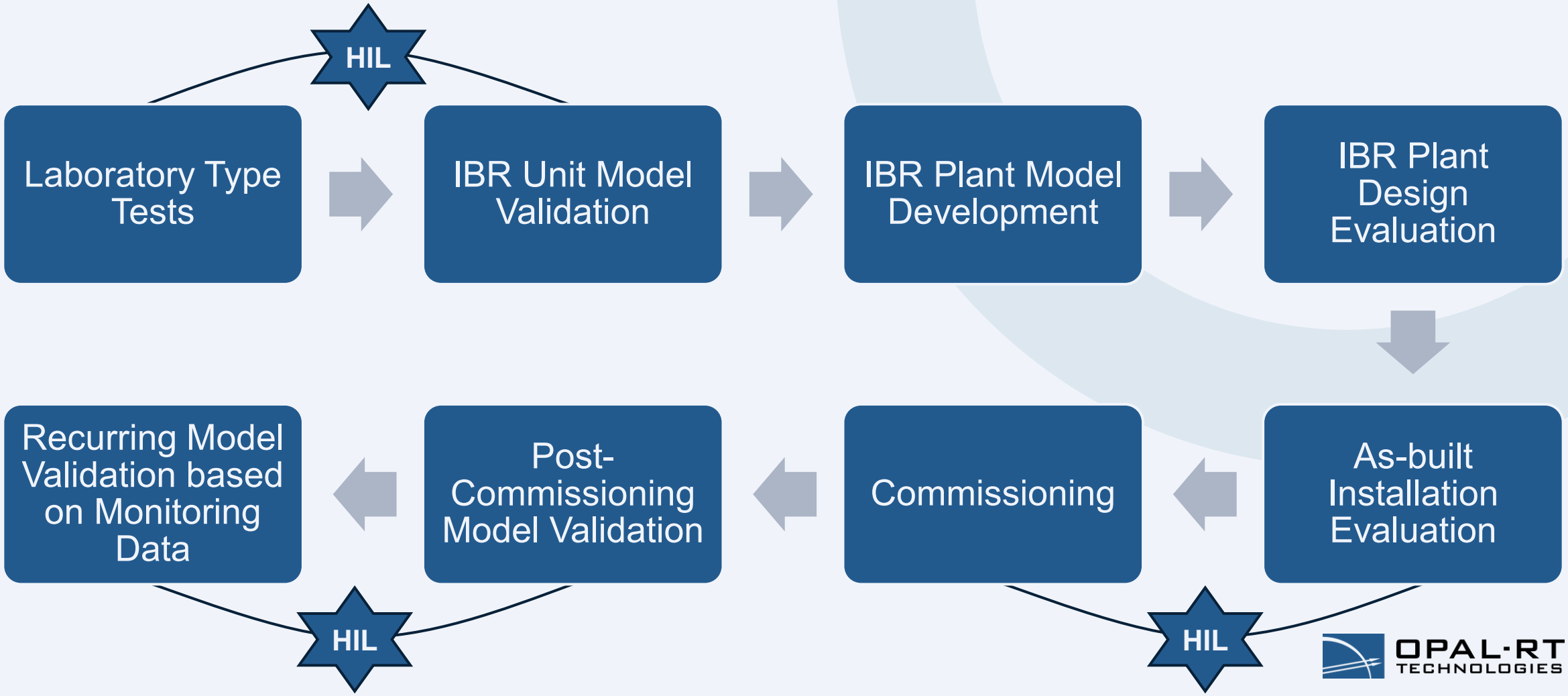
Role of HIL Testing in IEEE 2800 Conformity Assessment Process



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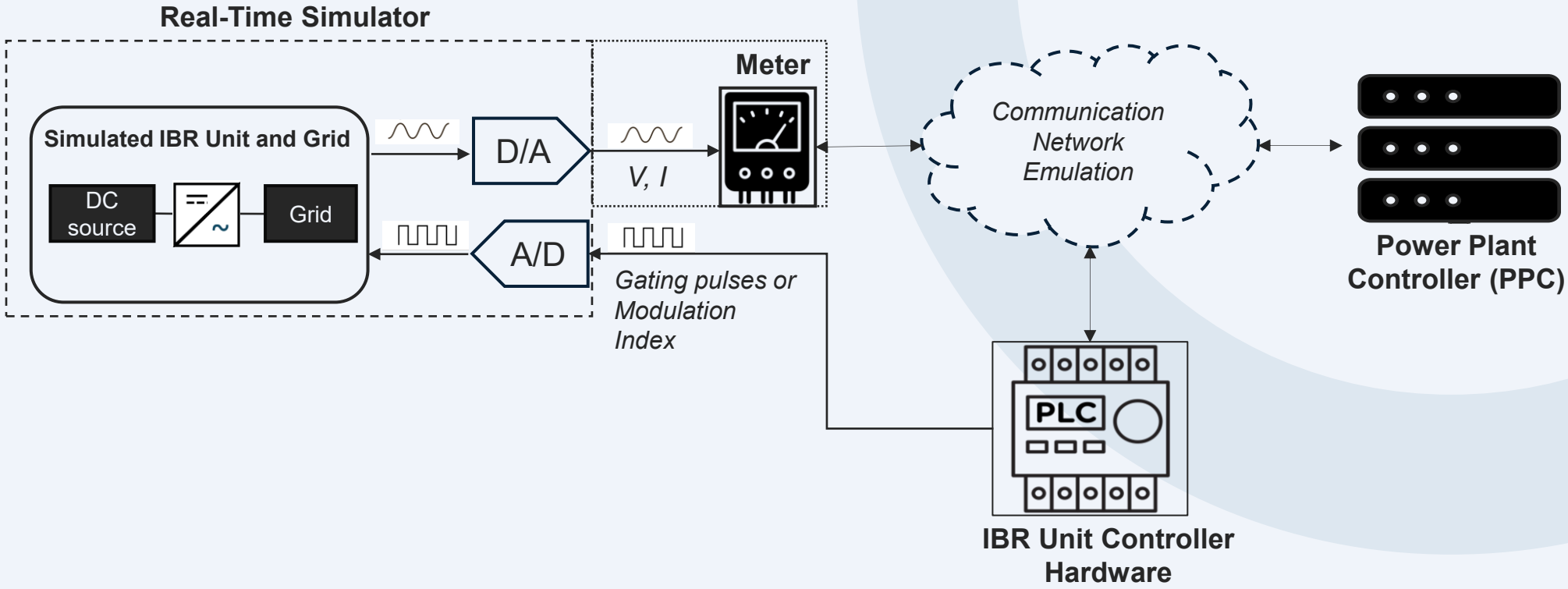
Controller Hardware in the Loop (CHIL) Testing – Generalized Architecture



IBR Unit Controller Model Validation

Protection/Ride-Through Behavior Testing

IBR Unit – PPC Coordination, Performance

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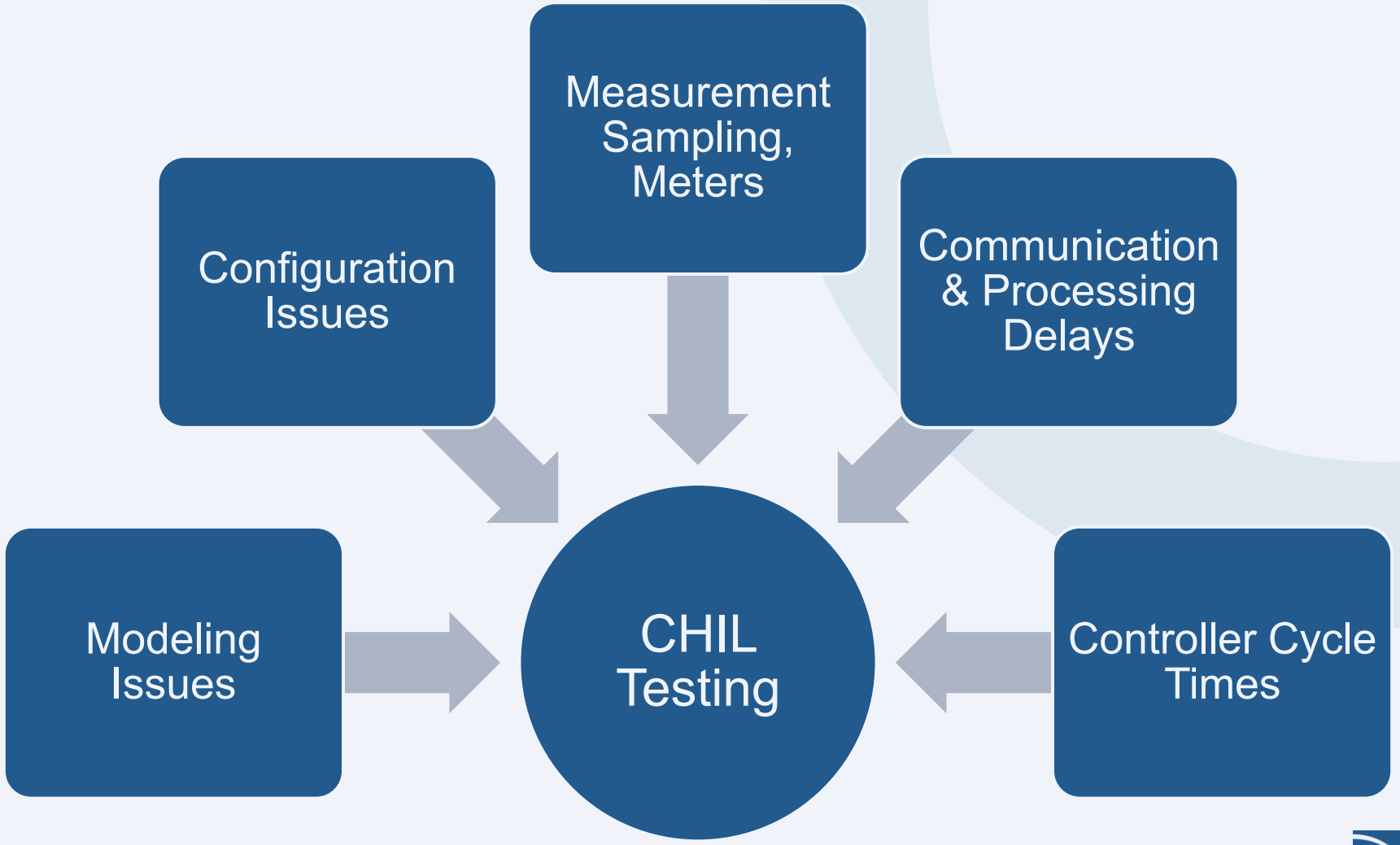
CHIL Testing Considerations for Model Validation



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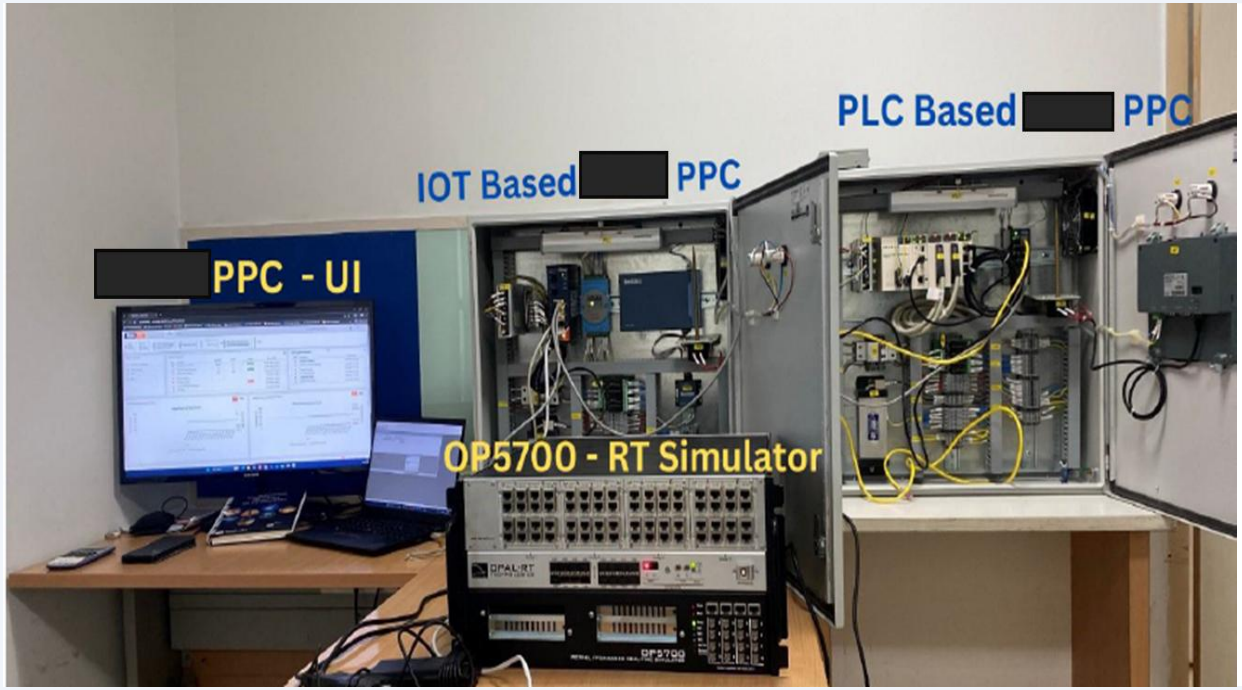
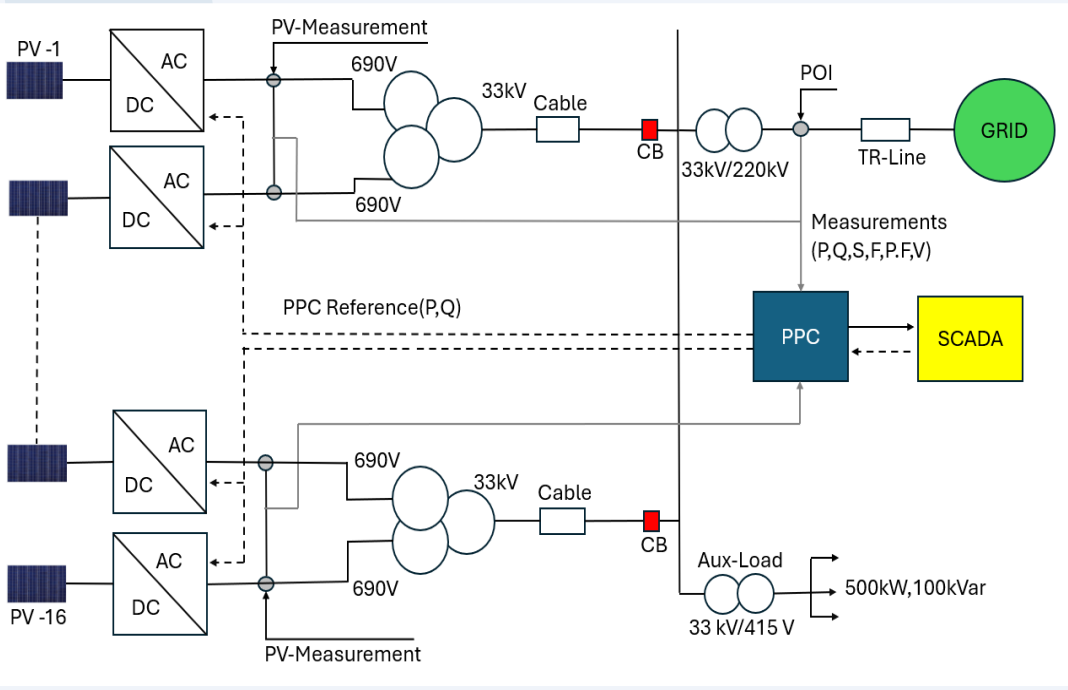
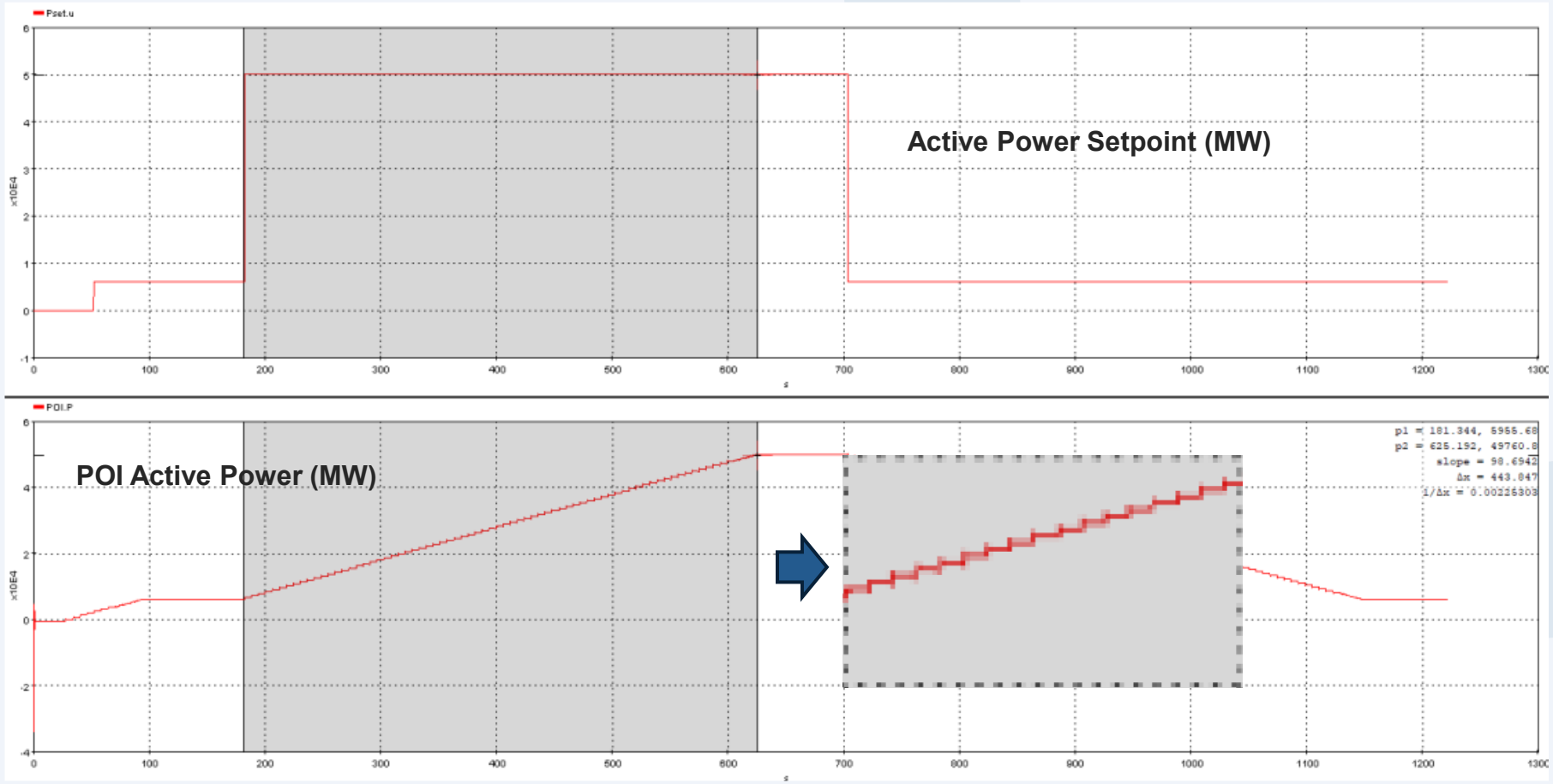
PPC CHIL Performance Testing – Test Setup and System Diagram

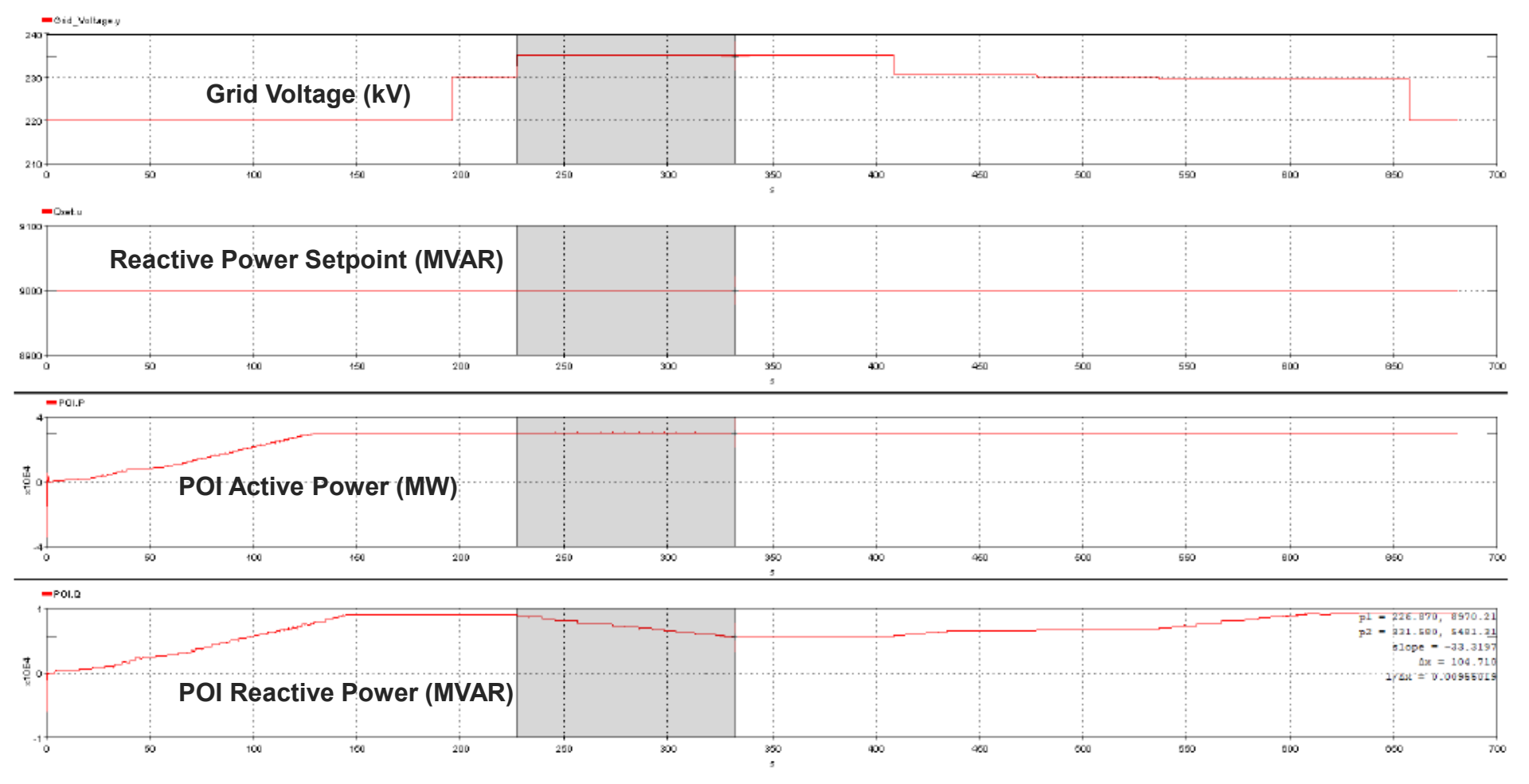




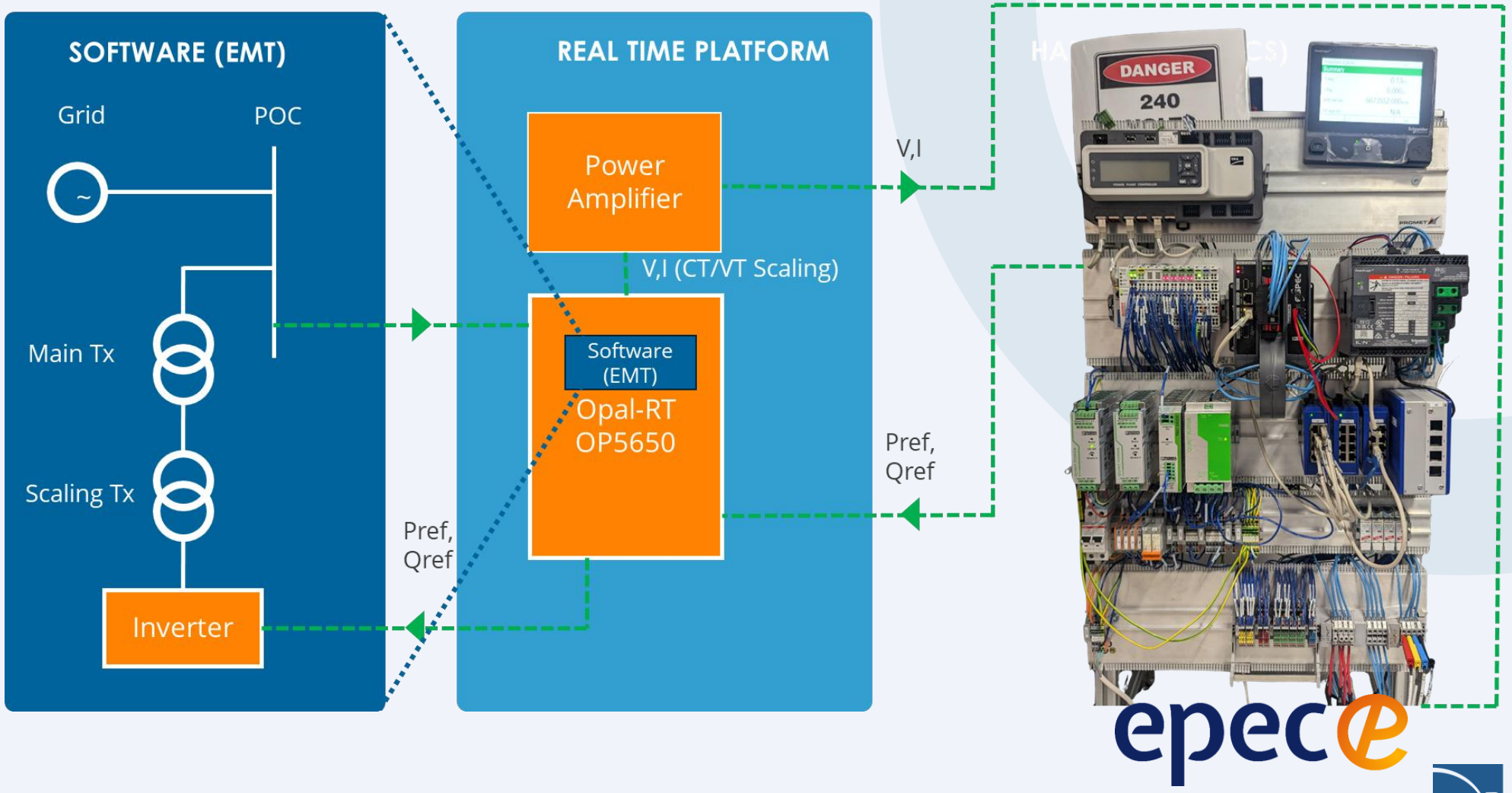
PPC CHIL Performance Testing – Active Power Ramp Test



PPC CHIL Performance Testing – High Voltage Response Test



Plant Level HIL Testing Pre-Commissioning Use Case



Source: Marty Johnson, EPEC Group presentation in OPAL-RT webinar titled 'USING HIL TO DERISK RENEWABLE PROJECT DELIVERY' https://www.opal-rt.com/power-in-mind/volume-8/article-2/

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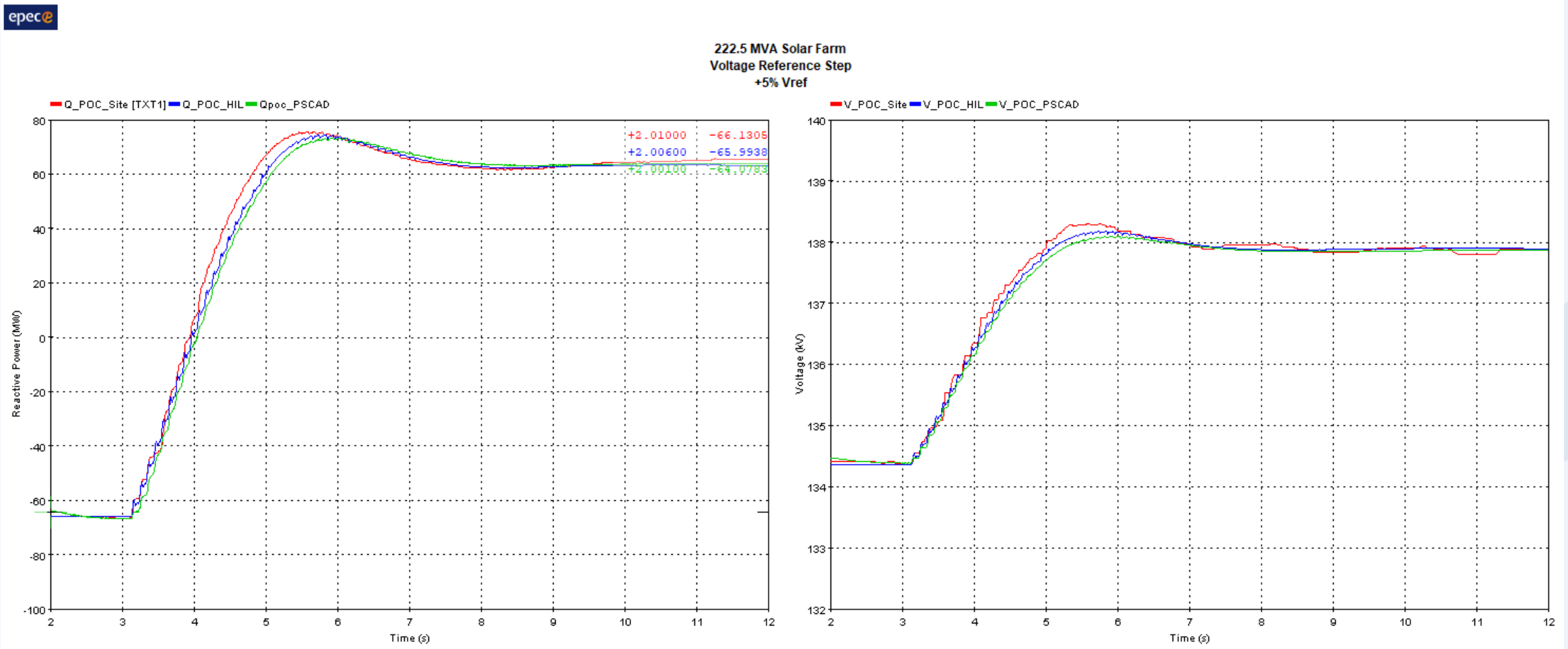

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Plant Level HIL Testing Pre-Commissioning Use Case

Real World Challenges Encountered and Addressed

- Controller hardware cycle time mismatch
- Delays due to metering configuration
- Failure to model equipment that added further delays
- PPC model vs. hardware mismatch
- Integration issues between vendor equipment
- Incorrect Frequency Measurements
- Variable Modbus Delays from Power Meters (30ms-200ms)
- Parameter conversion issues between model/equipment
- Identification of dynamic response issues from parameter mismatches
- Differing frequency responses with different PPC versions

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Conclusions

- Hardware in the Loop (HIL) Testing is essential to ensure validated unit-level as well as plant-level IBR models.
- HIL Testing is valuable in identifying various types of issues ranging from modeling errors or inadequacies, incorrect parameters, performance related issues including impact of communication protocols and delays.
- CHIL testing enables extensive testing of scenarios at various stages in the IBR plant lifecycle ranging from the initial stages to pre-commissioning as well as post-commissioning ensuring models are maintained properly.
- From an economical standpoint, they enable early identification of issues, leading to the derisking of project delivery and ensuring that commissioning delays are minimized, thereby minimizing penalties.

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Thank You

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