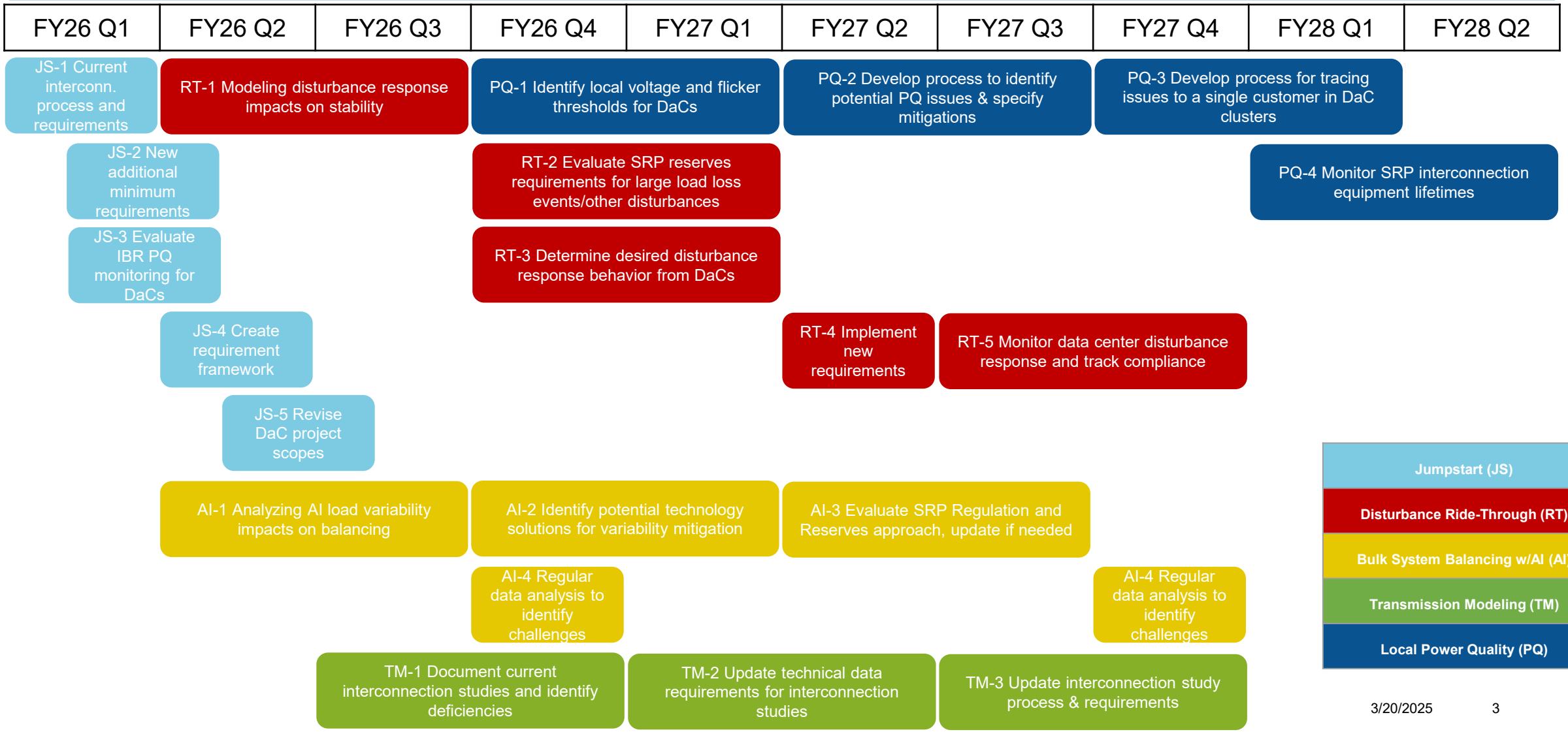
50 Years of Learning from Disturbance Ride-Through

Scott Anderson | 3-20-2025

Outline

- Setting the Stage
- 50 years of ride-through; CBEMA to IEEE 2800
- Deeper Focus on SEMI F47
  - What prompted it
  - What was developed
  - What were the results
  - Broader impacts
- Next steps for data centers?

SRP Data Center Readiness Strategy DRAFT

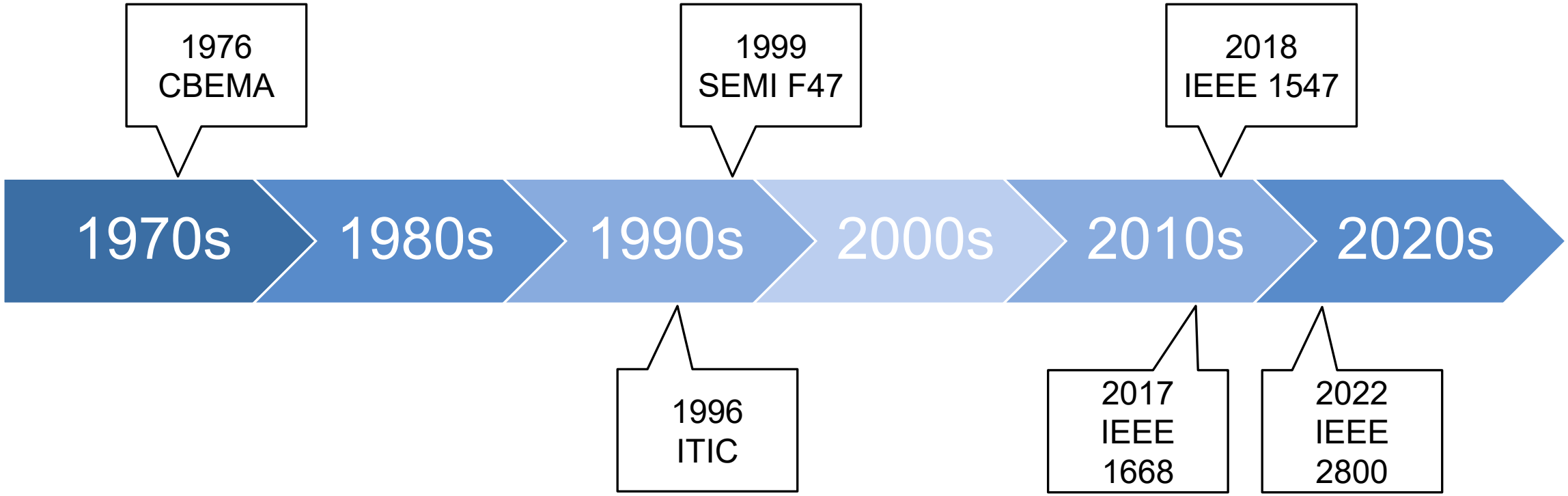


Eastern Interconnection Ride-Through Event July 10, 2024

- Lightning arrestor failed on a 230 kV system in Eastern Interconnect
- Auto-reclosing control was configured for three auto-recloses
- Six faults occurred over 82 seconds - all < 4 cycles, ranging from .25 to .40 Vpu
- Customer-initiated simultaneous loss of ~1500 MW of load
- Resulting in frequency and voltage increases, but not to levels risking reliability
- Not anticipated by the BA, but action was taken to reduce voltage

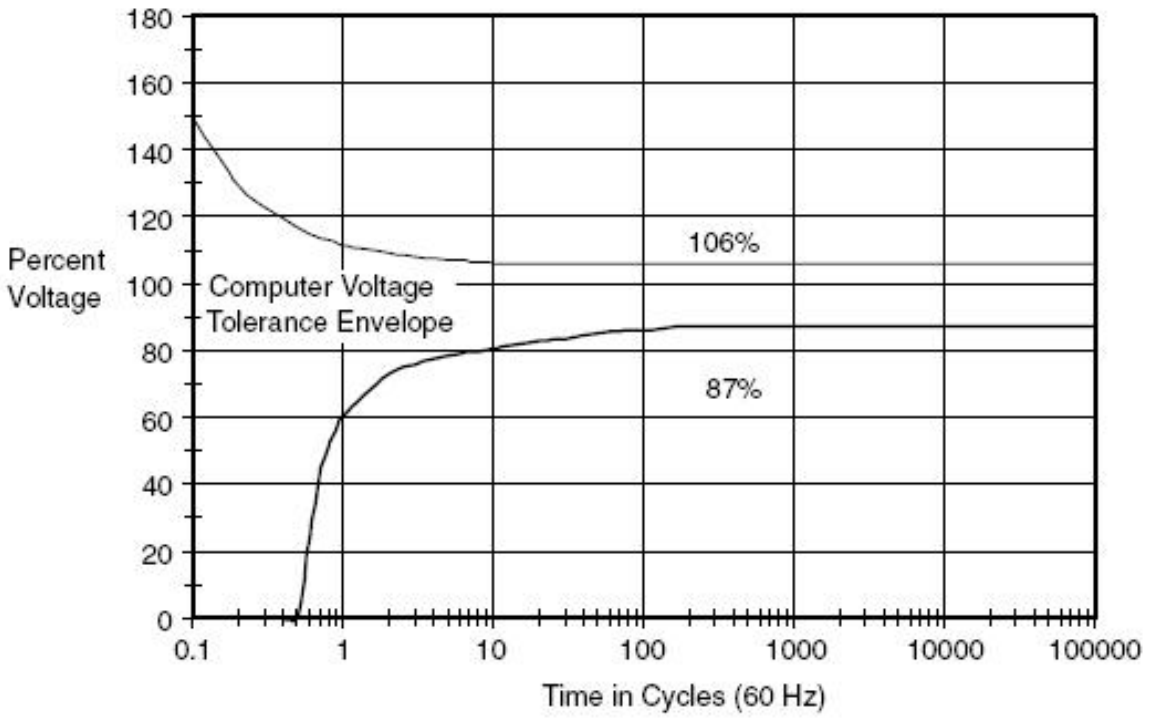
As the potential for this type of load loss increases, the risk for frequency and voltage issues also increases, and operators and planners should be prepared

50 Years of Addressing Disturbance Ride-Through



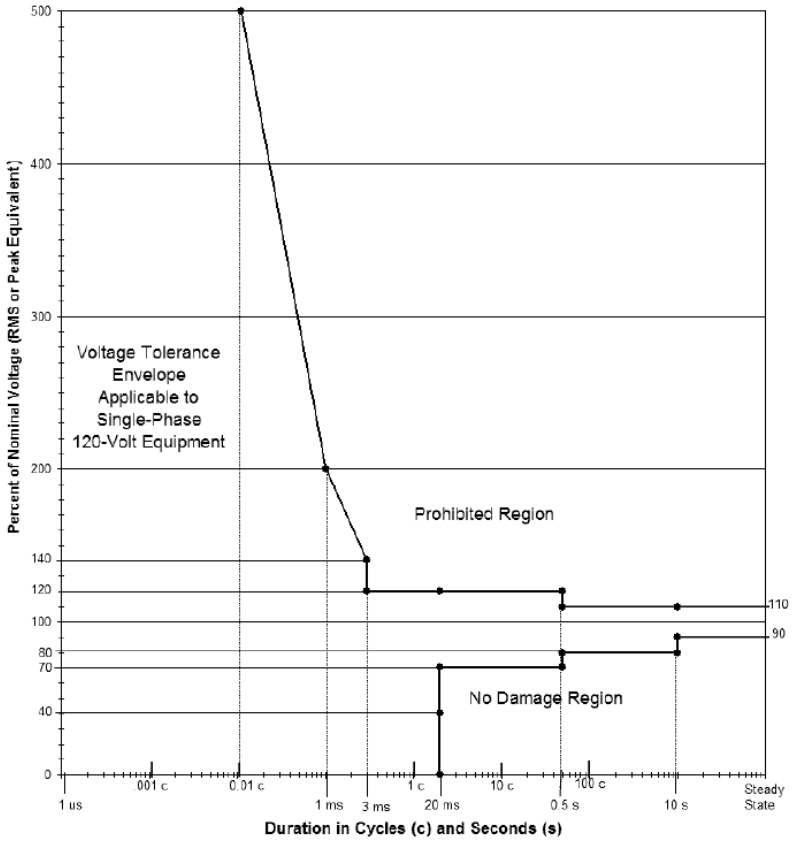
1977 CBEMA - Computer and Business Equipment Manufacturers Association

- **Purpose**: To define the power quality requirements for computer and business equipment
- **Voltage only**
- **Details**: The CBEMA curve describes the tolerance of IT equipment to voltage sags and swells



1996 ITIC - Information Technology Industry Council

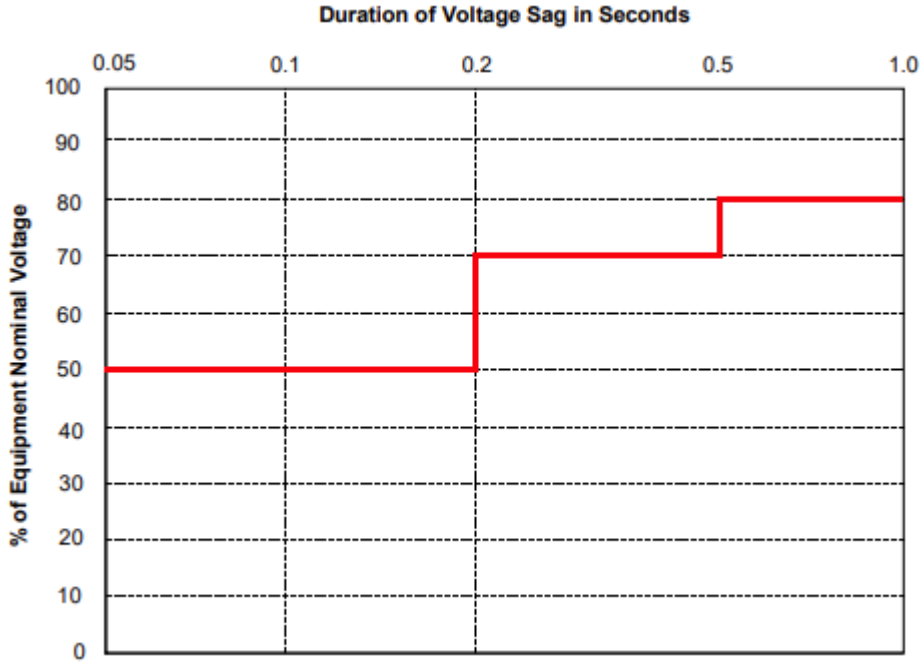
- **Purpose**: To provide an updated voltage tolerance curve for IT equipment
- **Voltage only**
- **Details**: The ITIC curve is an evolution of the CBEMA curve, focusing on modern IT equipment



From ITIC

1999 SEMI F47 Semiconductor Equipment and Materials Institute

- **Purpose**: To set voltage sag immunity standards for semiconductor manufacturing equipment.
- **Voltage Sag only**
- **Details**: SEMI F47 specifies the voltage sag ride-through capability required for semiconductor processing equipment



Excerpt from EPRI

SEMI is an international trade association representing semiconductor equipment and materials suppliers that develops standards for the semiconductor industry

What Prompted SEMI F47

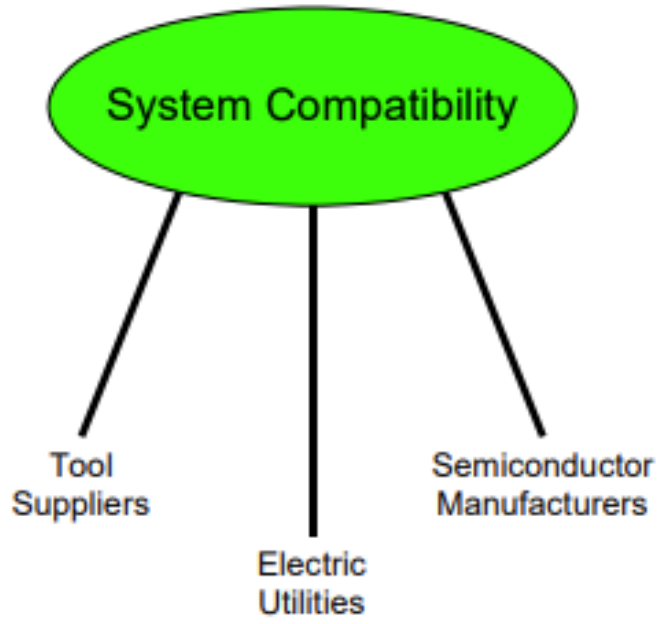
- Semiconductor industry was experiencing costly process interruptions and equipment shutdowns
- Expectations of customer was very high, including desiring perfect Power Quality
- Perfect Power Quality may not be achievable – What is achievable?

No.	Process	Reported Cost	Service Voltage	Load
1	Semiconductor	$1,500,000	69 kV	25 MW
2	Semiconductor	$1,400,000	161 kV	30 MW
3	Semiconductor	$ 700,000	12.5 kV	10 MW
4	Metal Casting	$ 200,000	13.8 kV	16 MW
5	Chemical Plant	$ 160,000	12.5 kV	5 MW
6	Pulp and Paper Mill	$ 110,000	161kV	100 MW
7	Aerospace Engine Machining	$ 100,000	13.8kV	10 MW
8	Food and Beverage	$ 87,000	12.5 kV	5 MW
9	Chemical Plant	$ 75,000	66kV	3 MW
10	Chemical Plant	$ 75,000	66kV	5 MW
11	Electronic Components	$ 75,000	12.5 kV	5 MW
12	Crystal Growth	$ 60,000	12.5 kV	1 MW
13	Chemical Plant	$ 46,175	66kV	30 MW
14	Wiring Manufacturing	$ 34,000	12.5 kV	2 MW
15	Chemical Plant	$ 18,000	12.5 kV	2 MW
16	Fibers Plant	$ 15,000	12.5 kV	1 MW
17	Paper and Packaging	$ 10,000	12.5 kV	4 MW
18	Plastic Bag Manufacturing	$ 10,000	480V	4 MW
19	Plastics	$ 7,500	12.5 kV	4 MW
20	Stainless Steel Manufacturing	$ 5,500	12.5 kV	2 MW

EPRI

How Was it Developed

- Started with a series of workshops from 1996-1999 led by EPRI
- The three-legged stool concept was born
- 1997 workshop led to the formation of a SEMI PQ Equipment Ride-Through Task Force focused on the following
    1. Review existing standards from IEEE, IEC, SEMI, CBEMA and others
    2. Review data from tools, facilities and utilities
    3. Developed voltage sag ride-through standards
    4. Develop a test methodology and power conditioning guideline



SEMI F47 Three-Legged Stool
Requires Buy-In and Collaboration from all

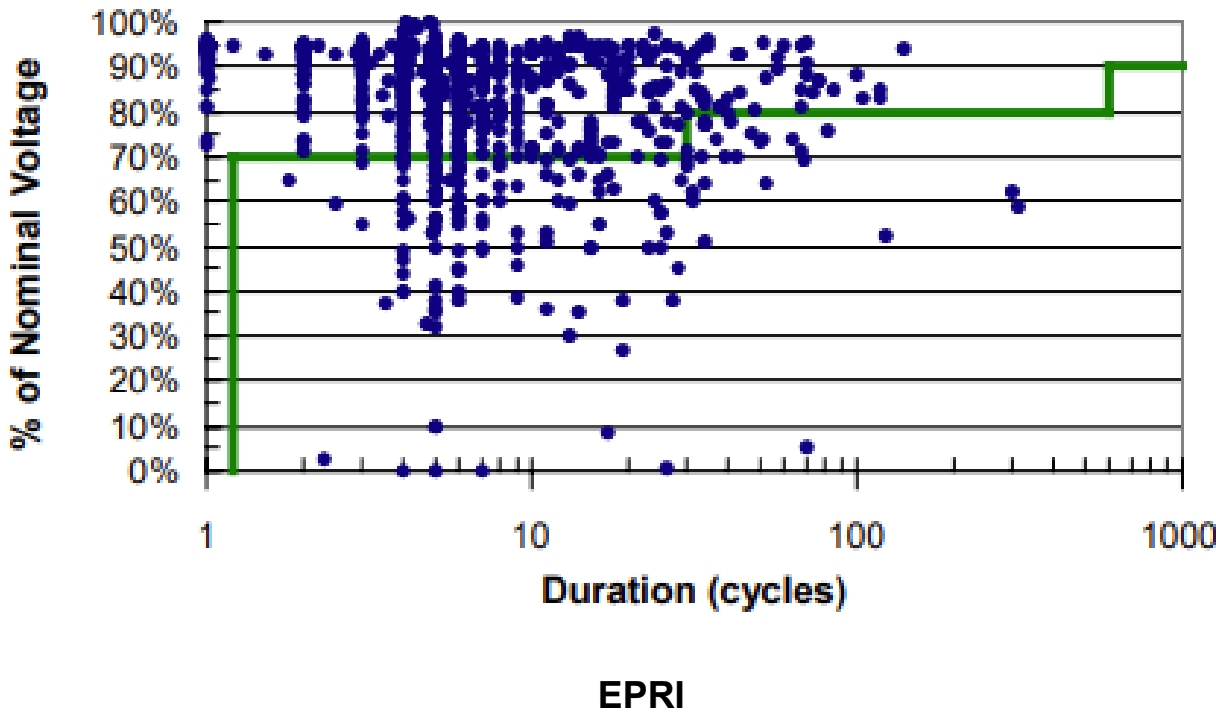
What Was Developed – All In 1999

Specifications

- SEMI F47 – *Semiconductor Processing Equipment Voltage Sag Immunity*
- SEMI F42 – Test Method for *Semiconductor Processing Equipment Voltage Sag Immunity*

Guidelines

- *Electric Utility Voltage Sag Performance for Semiconductor Factories*
- *Semiconductor Factories System Voltage Sag Immunity*



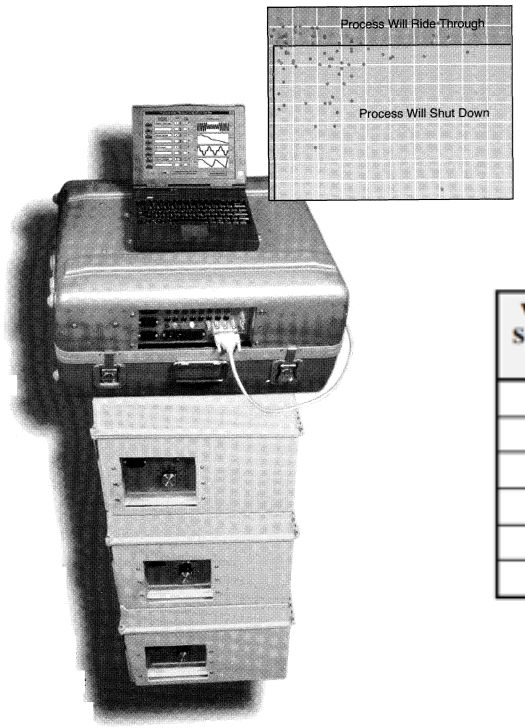
What Are the Results

- By implementing SEMI F47 semiconductor manufacturers improved tool reliability and improved uptime, in turn minimizing factory downtime and production losses
- This standard has become essential for ensuring the robustness of semiconductor processing equipment against common power quality issues
- Still in use today

Impact to the Industry was Much Broader than SEMI F47

- SEMI Standards were a big step; is it enough?
- SRP Started its PQ Services Group in 1996
  - An extra level of customer service
  - Consulting and investigations
  - PQ Training & Seminars
  - Voltage Sag Testing Program
  - Voltage Sag Mitigation Solutions
  - Power Quality monitoring

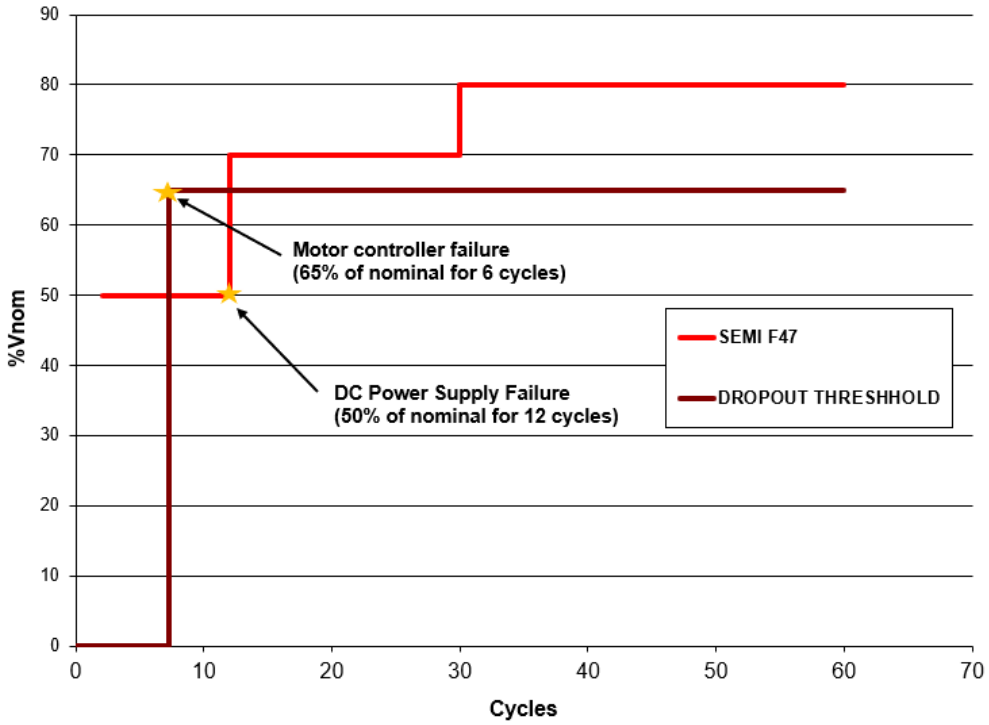
Voltage Sag Testing Program



Test Equipment

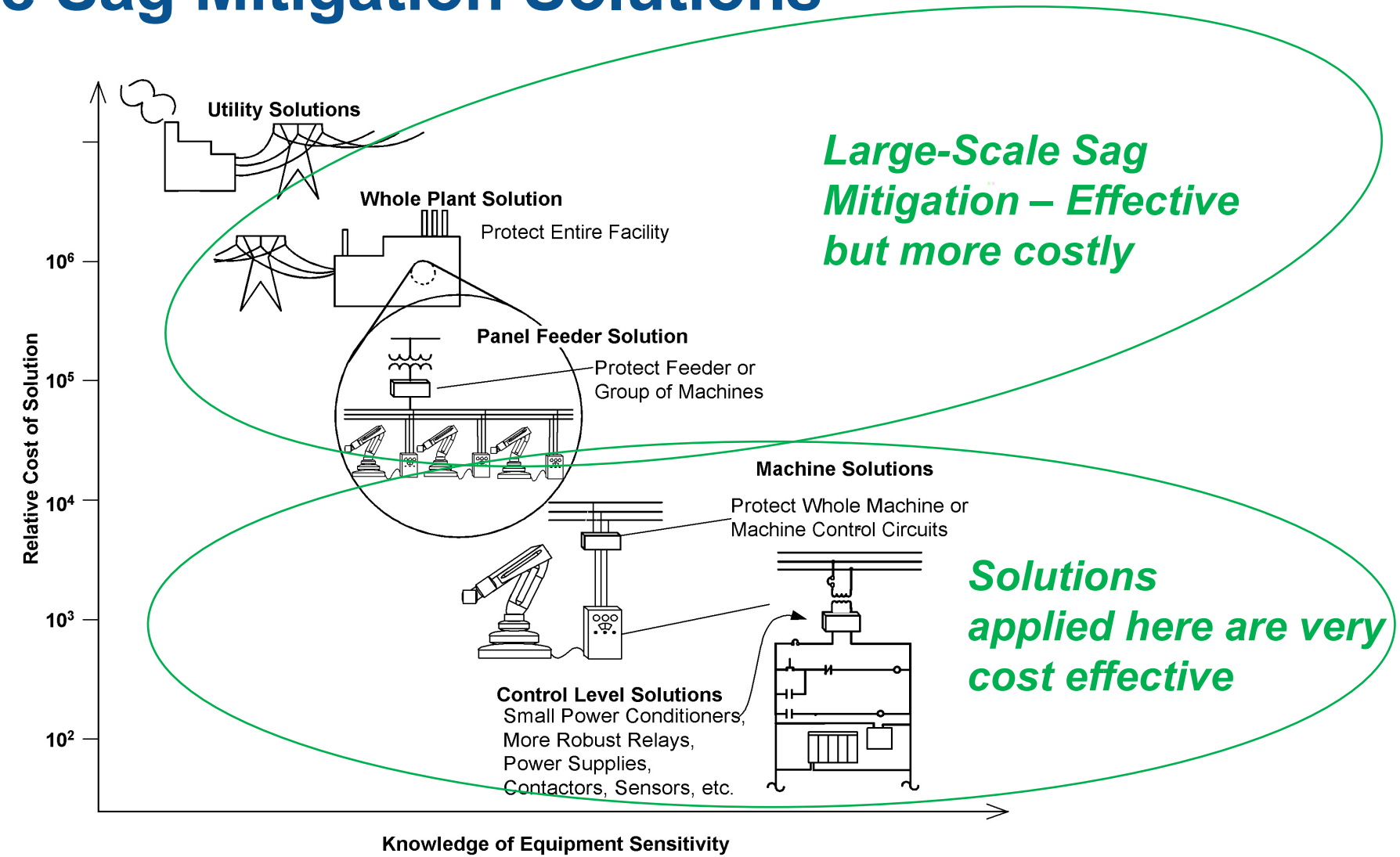
Voltage Sag Susceptibility Ranking	Weak Link	Overall %
1	EMO Circuit: Pilot Relay (33%) and Main Contactor (14%)	47%
2	DC Power Supplies: PC (7%), Controller (7%), I/O (5%)	19%
3	3 Phase Power Supplies: Magnetron (5%), RF (5%), Ion (2%)	12%
4	Vacuum Pumps	12%
5	Turbo Pumps	7%
6	AC Inverter Drives	2%

Testing Focus

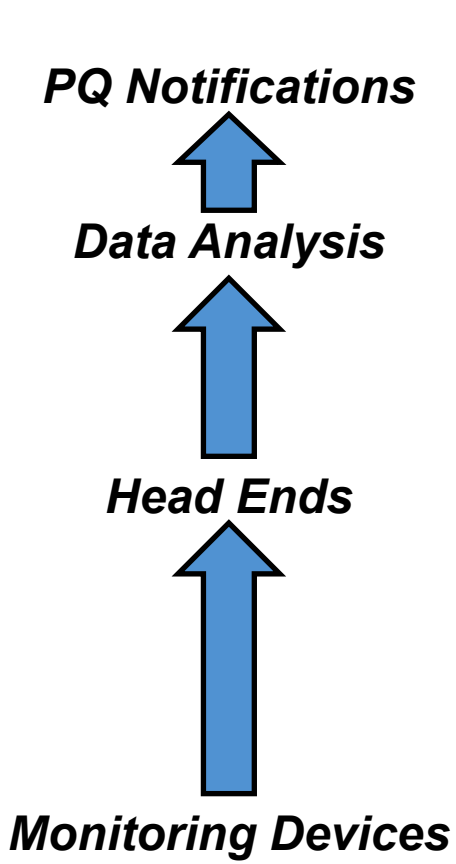


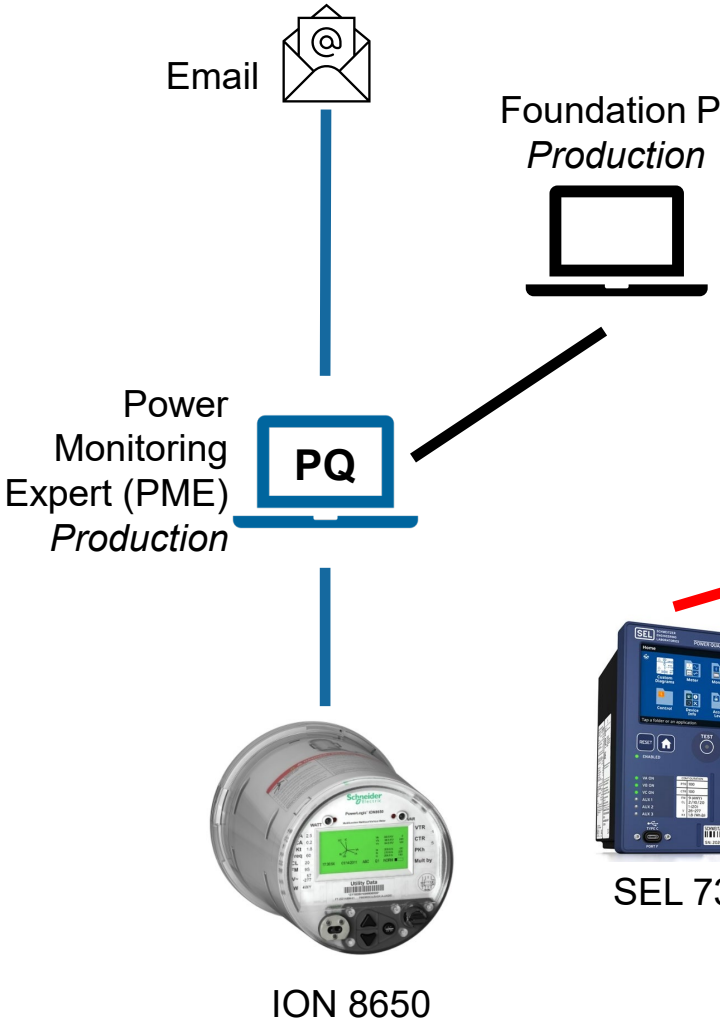
Test Results

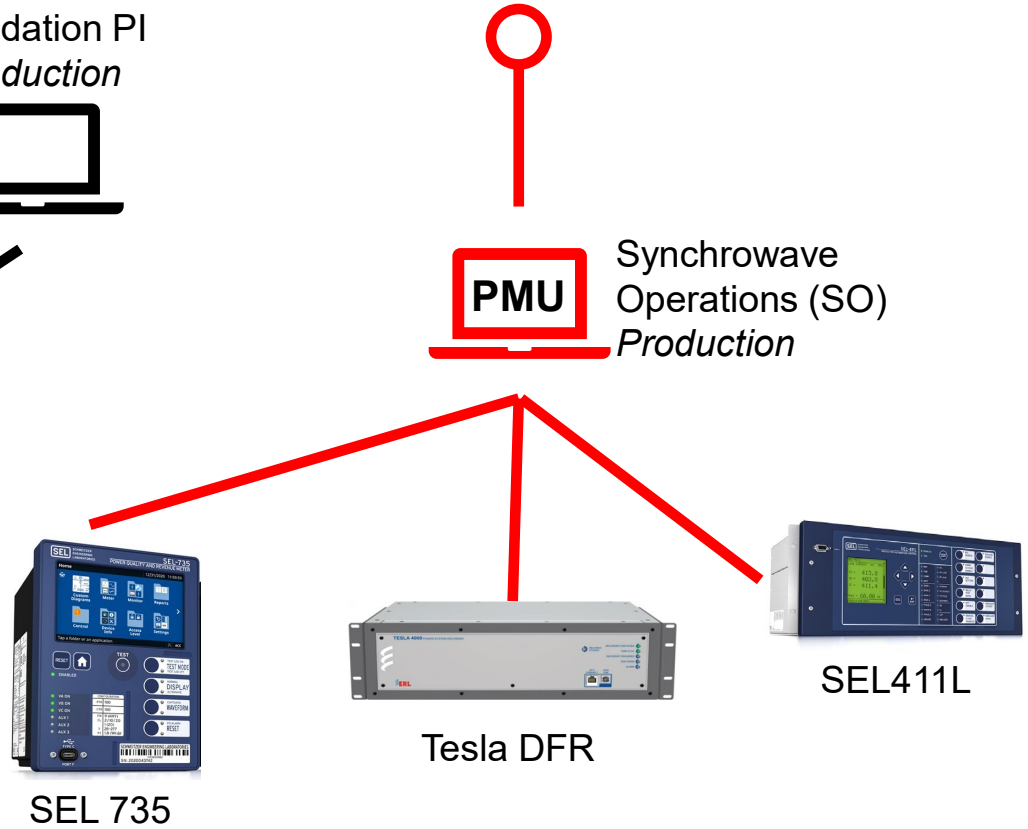
Voltage Sag Mitigation Solutions



Power Quality Monitoring

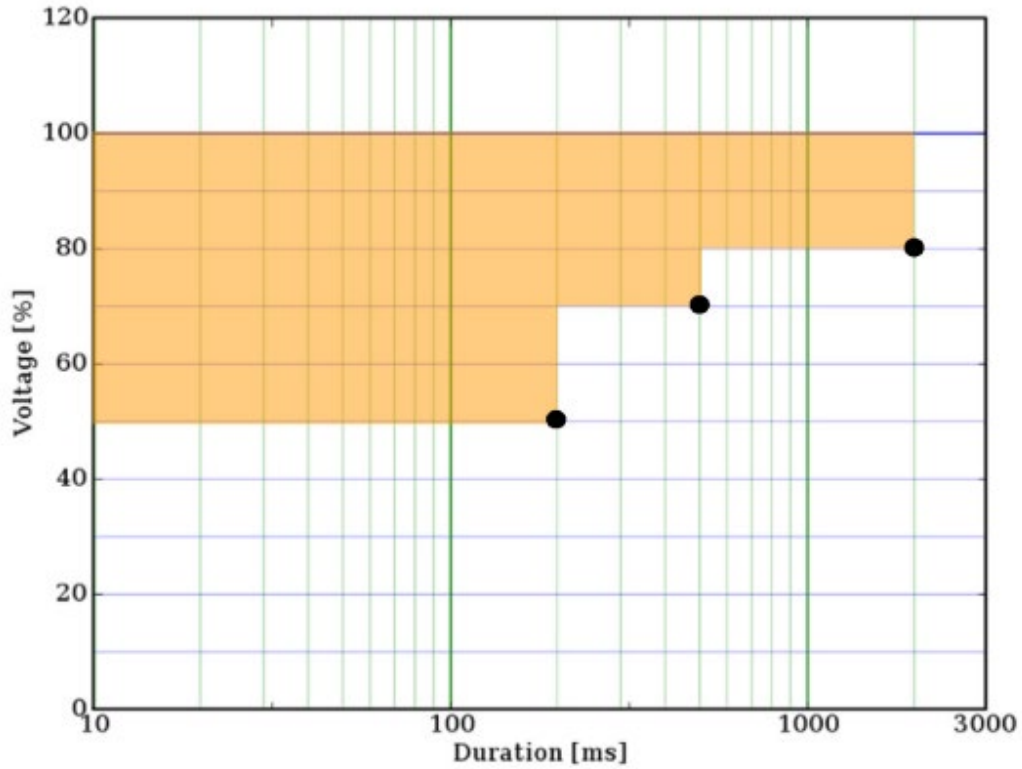






2017 IEEE 1668 Recommended Practice for Voltage Sag and Ride-Through Testing for End-Use Equipment

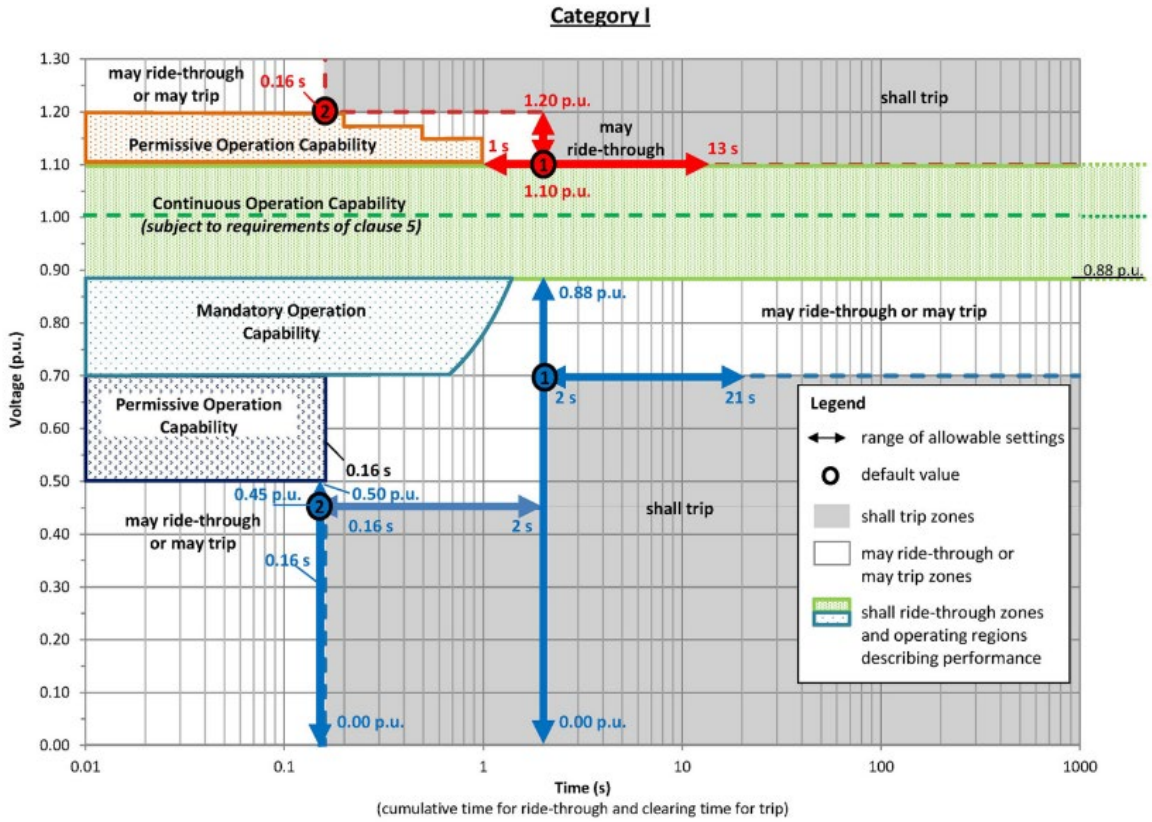
- **Purpose**: To provide recommended practices for voltage sag and short interruption ride-through testing for end-use electrical equipment.
- **Voltage Only**
- **Details**: This standard focuses on testing procedures and requirements for equipment connected to low-voltage power systems



Excerpt from IEEE 1668

2018 IEEE 1547 - Interconnection and Interoperability of Distributed Energy Resources with Power Systems

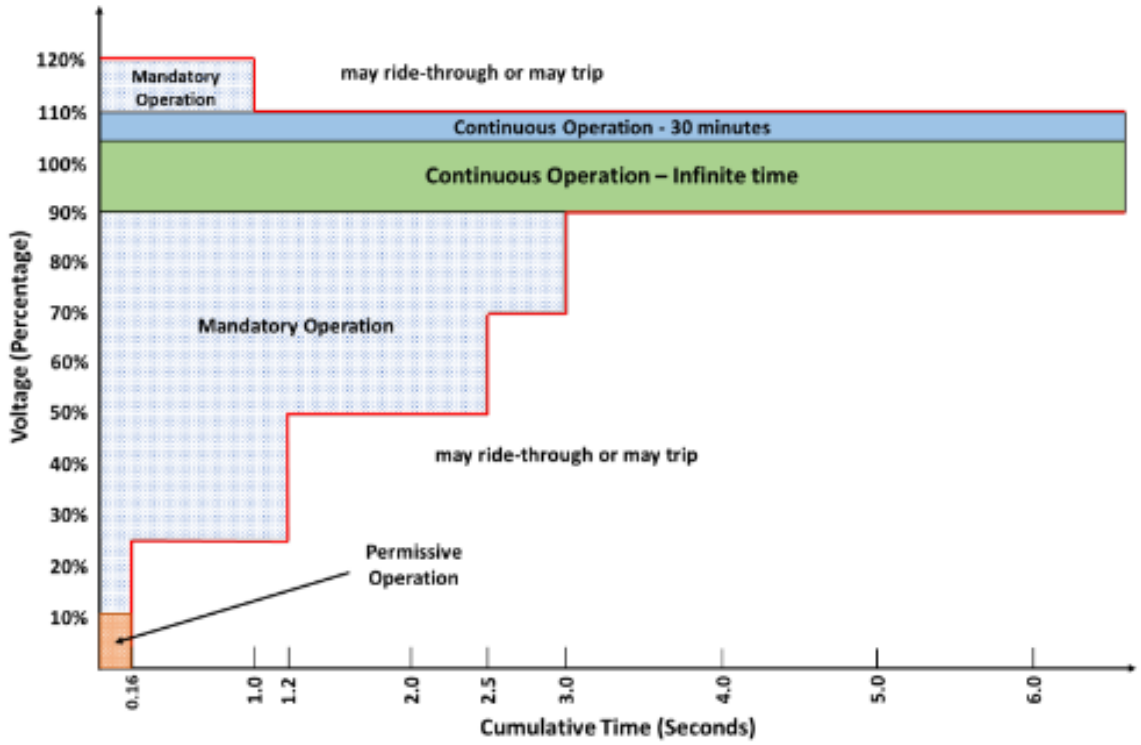
- **Purpose**: To establish interconnection and interoperability requirements for distributed energy resources (DERs)
- **Both voltage and frequency**
- **Details**: This standard includes low-voltage ride-through (LVRT) and frequency ride-through requirements for DERs



Excerpt from IEEE 1547

2022 - IEEE 2800 Interconnection and Interoperability of IBRs Interconnecting with Transmission

- **Purpose**: To define interconnection and interoperability requirements for inverter-based resources (IBRs) connected to transmission systems
- **Both voltage and frequency**
- **Details**: Addresses voltage and frequency ride-through capabilities and performance for transmission-connected IBRs

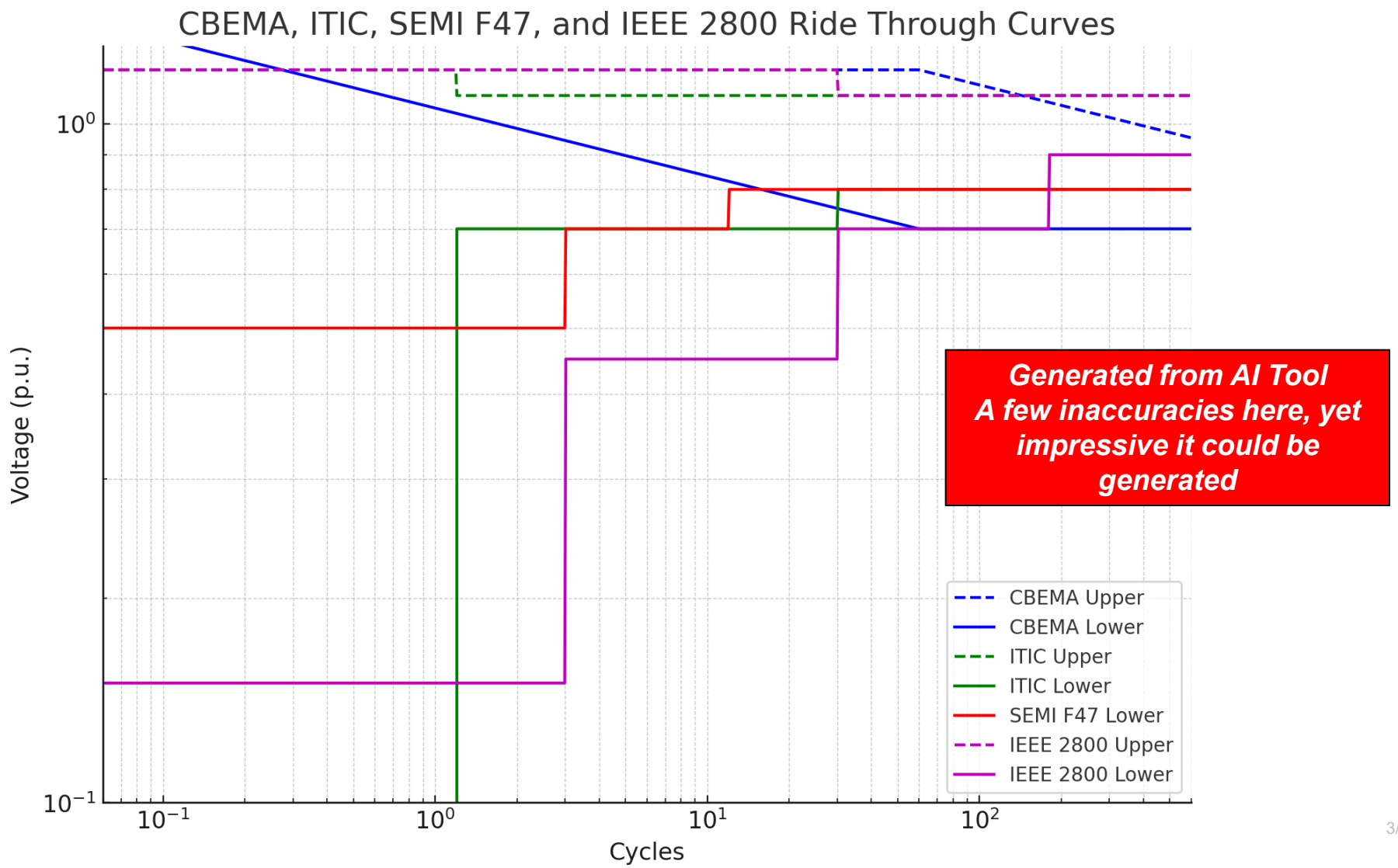


Excerpt from IEEE 2800

Comparison Table

Standard	Year	Purpose	VRT	FRT	Details
CBEMA	1977	Power quality requirements for computer and business equipment	Yes	No	Describes tolerance to voltage sags and swells
ITIC	1996	Updated voltage tolerance curve for IT equipment	Yes	No	Evolution of CBEMA curve, focusing on modern IT equipment
SEMI F47	1999	Voltage sag immunity for semiconductor manufacturing equipment	Yes	No	Specifies voltage sag ride-through capability for semiconductor processing equipment
IEEE 1668	2017	Recommended practices for voltage sag and short interruption ride-through testing	Yes	No	Focuses on testing procedures and requirements for low-voltage power systems
IEEE 1547	2018	Interconnection and interoperability requirements for DERs	Yes	Yes	Includes LVRT and frequency ride-through requirements for DERs
IEEE 2800	2022	Interconnection and interoperability requirements for IBRs	Yes	Yes	Addresses voltage and frequency ride-through capabilities and performance for transmission-connected IBRs

Comparison of Voltage Ride-Through - Developed by AI



Generated from AI Tool
A few inaccuracies here, yet impressive it could be generated

Next Steps

- What we have learned
  - We have been here before!
  - We know we can solve this!
- What can we apply to data centers?
  - Is a new ride-through standard needed?
  - Can an existing standard be used?
  - Should IT Loads & Facility Systems be separate?
  - Should solutions be GPU focused or site-wide?
  - What ride-through scenarios should be considered?

Table A

Root-Mean-Square Voltage (p.u. of nominal)	Minimum Ride-Through Time (seconds)
V > 1.20	May ride-through or trip
1.10 < V ≤ 1.20	0.5
0.90 ≤ V ≤ 1.10	Continuous
0.80 ≤ V < 0.90	2.0
0.70 ≤ V < 0.80	0.50
0.50 ≤ V < 0.70	0.20
V < 0.50	0.15

Table B

Instantaneous Phase-to-Phase or Phase-to-Ground Voltage (p.u. of nominal)	Minimum Ride-Through Time (milliseconds)
V > 1.80	May ride-through or trip
1.70 < V ≤ 1.80	0.2
1.60 < V ≤ 1.70	1.0
1.40 < V ≤ 1.60	3.0
1.20 < V ≤ 1.40	15.0

From ITIC Curve

Based on IEEE 1668 Single-Phase and Phase-Phase Curve

Based on ITIC Curve, but extended to ride-through fault duration

Excerpt from ERCOT Presentation on NOGRR245

thank you!

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